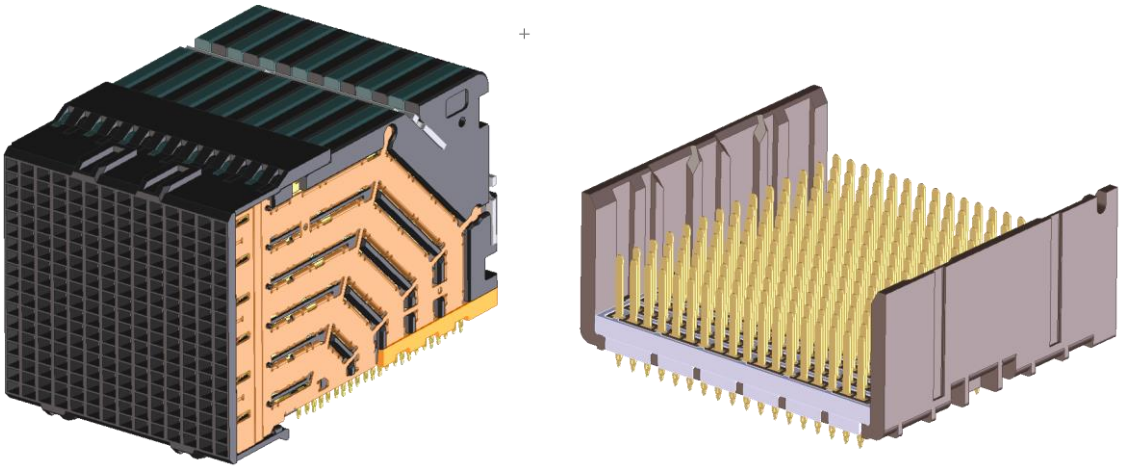
CONNECTOR ROUTING GUIDE

Impact™

Impact zX2 Backplane System
Connector Routing Guide



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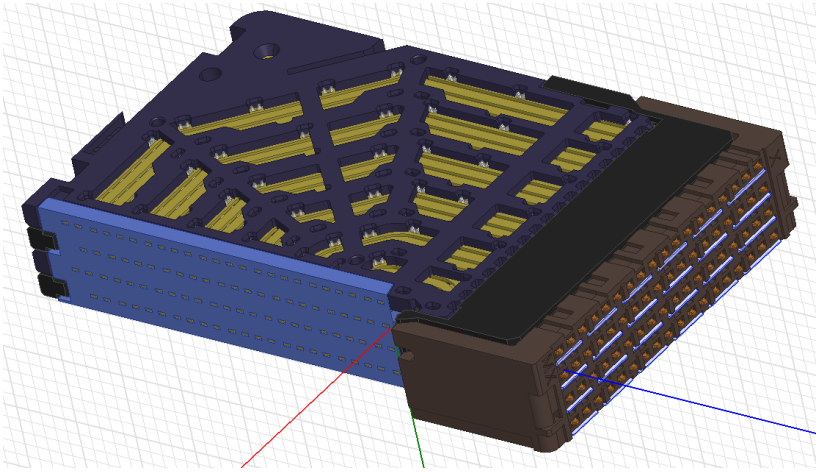
I. OVERVIEW OF THE CONNECTOR

The Impact zX2 backplane connector system provides data rates up to 28 Gbps and superior signal density up to 80 differential pairs per inch. The Impact zX2 System's broad-edge-coupled technology enables low cross-talk and high signal bandwidth while minimizing channel performance variation across every differential pair within the system.

The Impact zX2 backplane connector system is designed for traditional backplane and/or midplane architectures to meet the growing demands of next-generation telecommunication and data networking equipment manufacturers. The Impact zX2 backplane connector system is offered from 2 pair to 6 pair BP header and DC connector versions.



reference for 6 pair BP header and DC connector versions

II. ROUTING STRATEGIES

A) Compliant Pin Via Constructions

The Impact zX2 backplane header is designed for 0.36mm diameter plated-thru-holes. The backplane hole pattern changes for the different compliant pin sizes in order to optimize the signal integrity performance. Figures 1 and 2 illustrate the daughtercard and backplane hole patterns. (Please reference the appropriate sales drawings for the fully dimensioned hole patterns.)

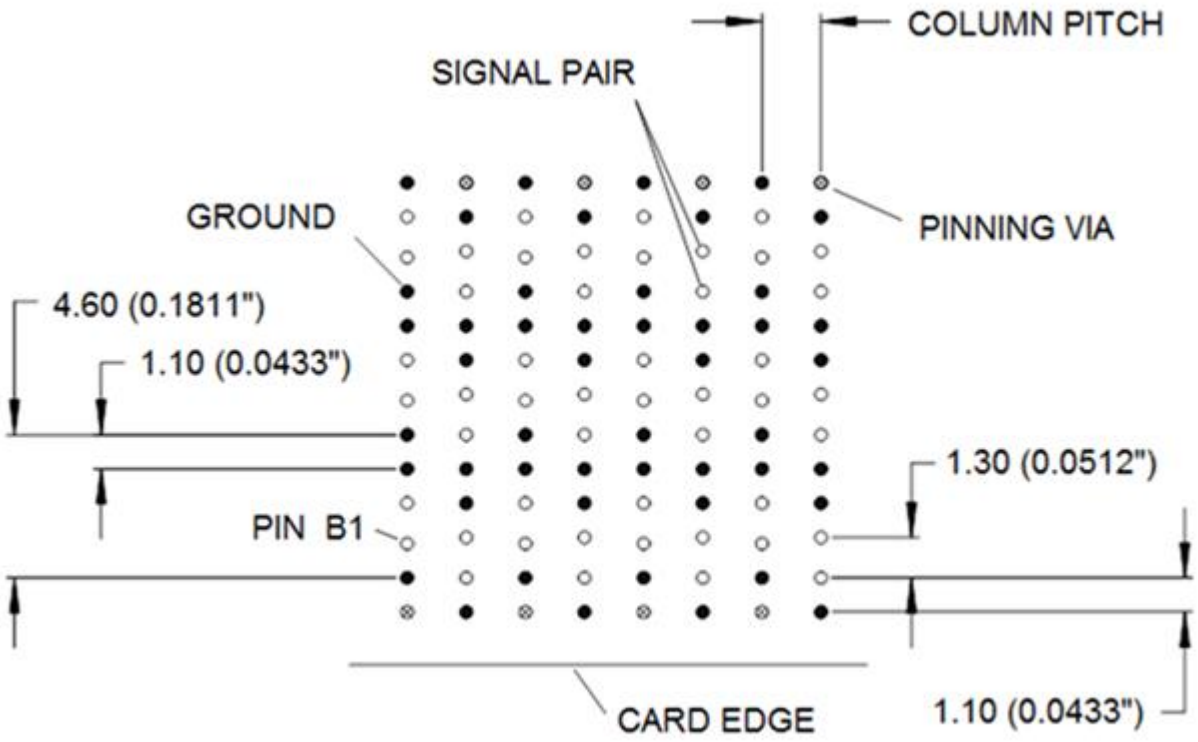


Figure 1
8 Column zX2 Daughtercard Hole Pattern

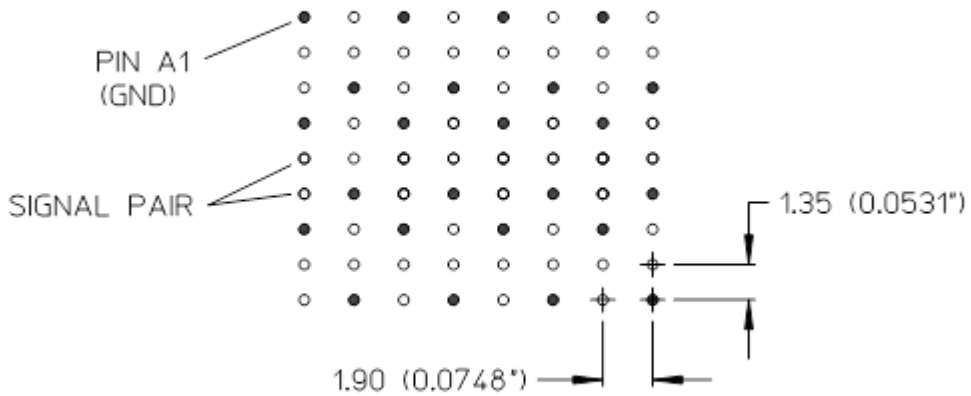
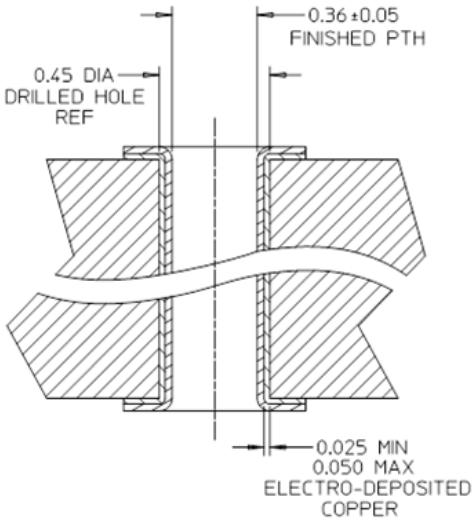


Figure 2
8 Column zX2 Backplane Hole Pattern

Refer to the appropriate Sales Drawing for the recommended PCB thickness



Notes:

1. The finished pcb hole size is the critical feature for proper performance of the compliant pin terminal. The reference drill sizes listed are recommended based on Molex's qualification to achieve the finished pcb hole size. It is important to maintain a reasonable Cpk to this feature.
2. Depending upon the specific manufacturer's plating process, a different drill size can be used to achieve the required finished pcb hole size.
3. The typical drill hole tolerance is +/-0.013mm.

The recommended pad stack for the two hole sizes are contained in Table A. All non-functional pads are to be removed for high speed applications.

FEATURE	0.36mm PTH NOMINAL DIA
Finished hole	0.36mm (14.2 mil)
Drill (REF)	0.45mm (17.7 mil)
Interior Pad	0.70mm (27.6 mil)
Top Layer Pad	0.70mm (27.6 mil)
Bottom Layer Pad	0.70mm (27.6 mil)
Anti-pad	See Figure 3 &4

Table A
Pad Stack Dimensions

B) Transmission Line Configuration

Coupled differential strip lines are the recommended transmission lines for high speed applications. For a specific system differential impedance (i.e., 100), different trace width and spacing can be accommodated for any preferred pcb stack up configuration. Designers often consider particular common mode impedance based on factors such as skew, fabrication consistency, and density. Any particular choice of trace width and spacing ultimately affects the routing configuration within the routing channel. In high speed applications, the routing channel is a defined channel between the connector column pins.

C) Anti-pad Size

For most high-speed applications, one needs to maximize the anti-pad width (between columns) and length (between rows). The width of the anti-pad is affected by the following:

1) Trace width and spacing
2) Pair to pair spacing
3) Top and bottom ground strips to trace edge spacing

The length of the anti-pad is limited by the distance and the construction of ground pin vias. The anti-pads shown in Figures 3 and 4 are based on a 7 mil trace width and spacing and a 4 mil registration buffer (top and bottom ground strips edge to trace outer edge).

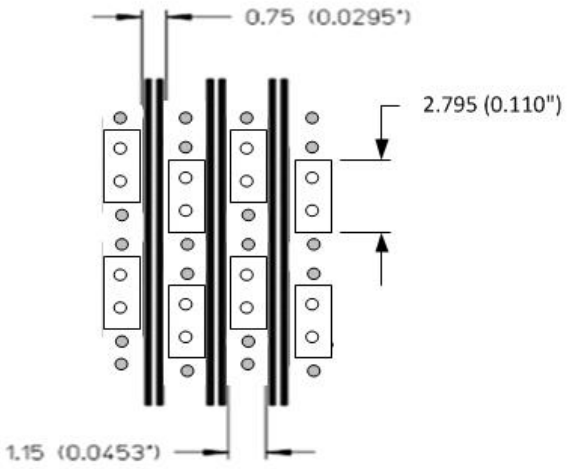


Figure 3
zX2 Daughtercard Anti-Pad Size

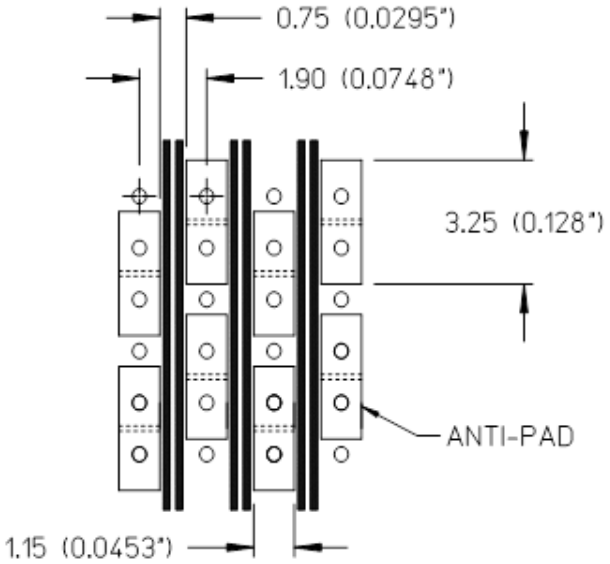


Figure 4
zX2 Backplane Anti-Pad Size

D) Differential Trace to Signal Pad Attachment

There are several ways to connect the differential traces to their corresponding signal pads. Two possible methods are illustrated in Figures 5 and 6.

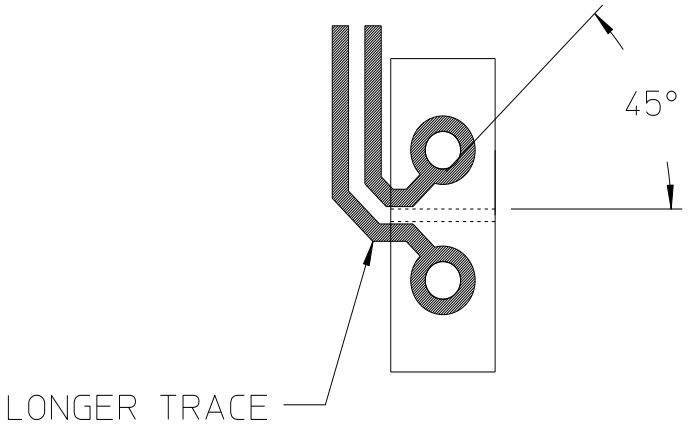


Figure 5
Standard Escape Detail

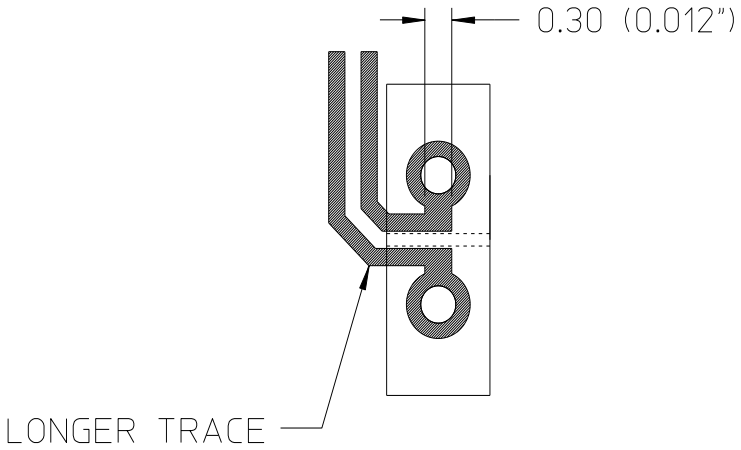


Figure 6
Flag Escape Detail

As seen in Figures 5 and 6, one of the traces has a longer length than the other one. This uneven length should be corrected to reduce the skew within the channel.

III. CROSSTALK

Crosstalk mitigation is a critical element of high speed system design. There are some simple considerations to reduce crosstalk in many systems. These include the following:

1. Separate transmit and receive transmission lines. If transmit and receive transmission lines need to be placed on the same layer, separate them with extra space. It is recommended to place them on separate routing layers.
2. Separate transmit and receive vias. Group the TX and RX differential vias in blocks in rows or columns and, if possible, separate them with slow or DC signal lines.

Tables C and D show two examples of TX and RX grouping.

	1	2	3	4	5	6	7	8	9	10
A	G	TX	G	TX	G	LS	G	RX	G	RX
B	TX	TX	TX	TX	LS	LS	RX	RX	RX	RX
C	TX	G	TX	G	LS	G	RX	G	RX	G
D	G	TX	G	TX	G	LS	G	RX	G	RX
E	TX	TX	TX	TX	LS	LS	RX	RX	RX	RX
F	TX	G	TX	G	LS	G	RX	G	RX	G
G	G	TX	G	TX	G	LS	G	RX	G	RX
H	TX	TX	TX	TX	LS	LS	RX	RX	RX	RX
J	TX	G	TX	G	LS	G	RX	G	RX	G
K	G	TX	G	TX	G	LS	G	RX	G	RX
L	TX	TX	TX	TX	LS	LS	RX	RX	RX	RX
M	TX	G	TX	G	LS	G	RX	G	RX	G

Table C

TX RX grouping separated by low speed (LS) signal columns

	1	2	3	4	5	6	7	8	9	10
A	G	TX	G	TX	G	TX	G	TX	G	TX
B	TX	TX	TX	TX	TX	TX	TX	TX	TX	TX
C	TX	G	TX	G	TX	G	TX	G	TX	G
D	G	TX	G	TX	G	TX	G	TX	G	TX
E	TX	TX	TX	TX	TX	TX	TX	TX	TX	TX
F	TX	G	TX	G	TX	G	TX	G	TX	G
G	G	RX	G	RX	G	RX	G	RX	G	RX
H	RX	RX	RX	RX	RX	RX	RX	RX	RX	RX
J	RX	G	RX	G	RX	G	RX	G	RX	G
K	G	RX	G	RX	G	RX	G	RX	G	RX
L	RX	RX	RX	RX	RX	RX	RX	RX	RX	RX
M	RX	G	RX	G	RX	G	RX	G	RX	G

Table D

TX RX grouping by columns (separated by defined shields)

IV. BACKDRILLING

For high speed signals, it may be necessary to remove excess via stub below the pcb signal layer. This is accomplished by backdrilling the plated via with a larger diameter drill to remove the undesirable excess via, The Impact zX2 compliant pin design allows for backdrilling to within 1mm of the top surface of the pcb.

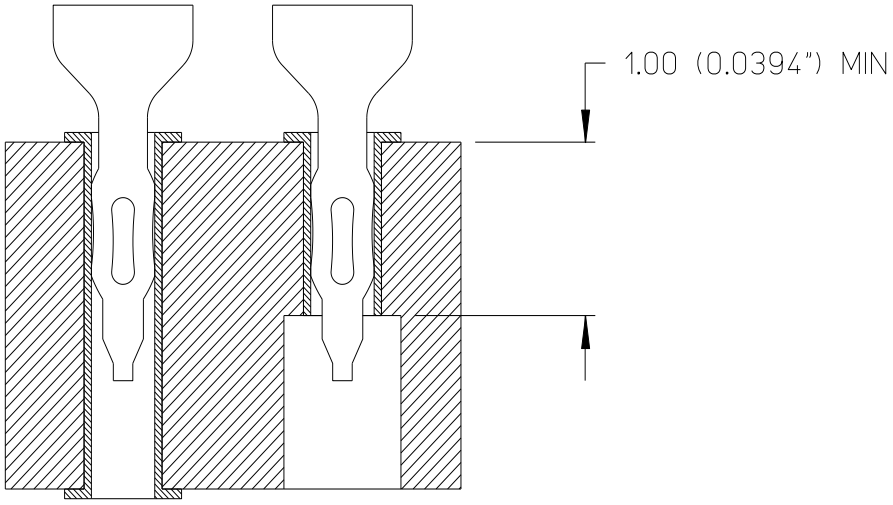


Figure 7
Backdrill Specification