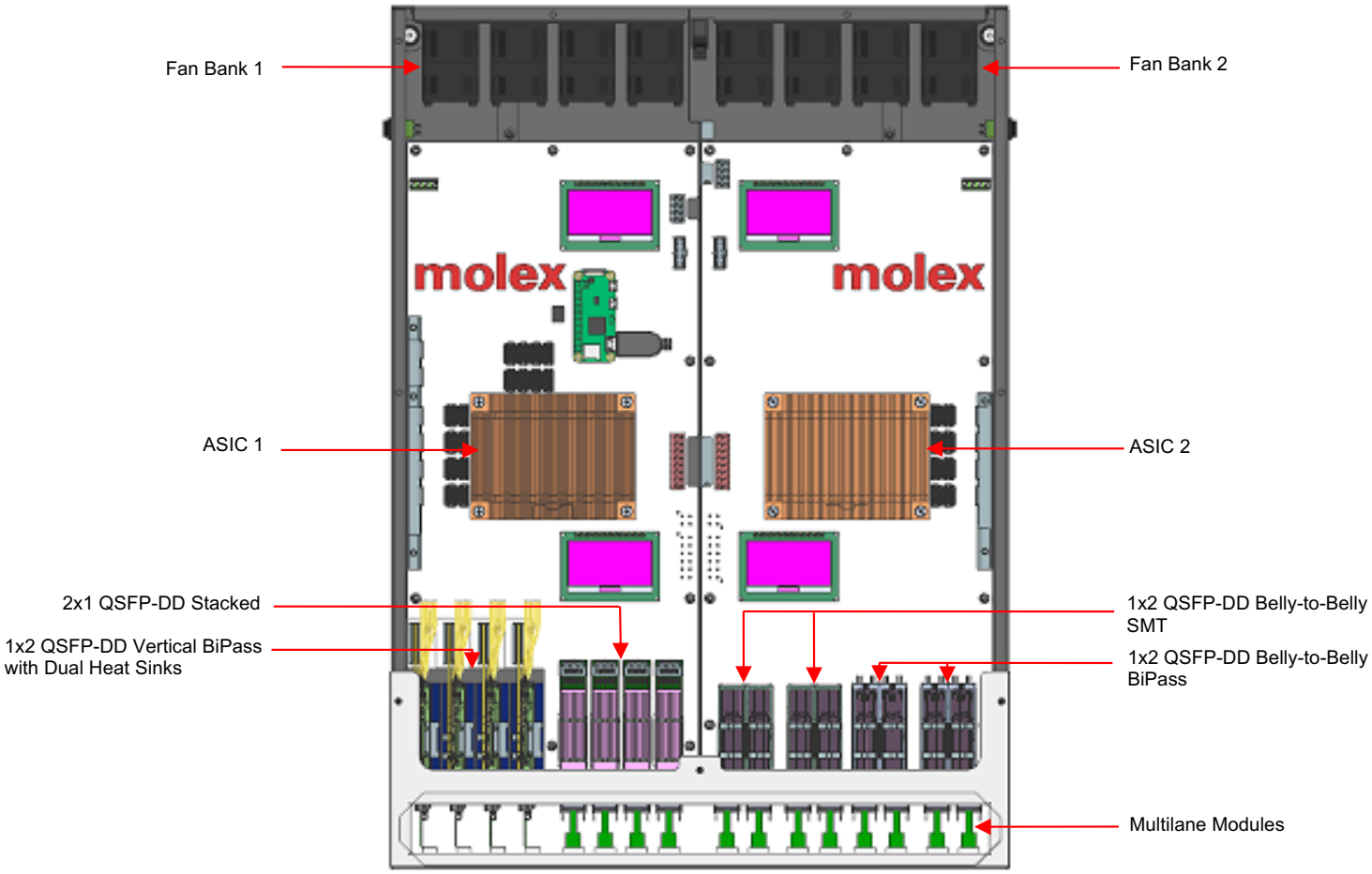
THERMAL DEMO FOR DESIGNCON



Thermal Demo - Top Down View

1. OBJECTIVE

The main objective of this thermal demo was to highlight the cooling capabilities of four different Molex cage products for QSFP-DD.

2. DATA

2.1 MODULE CASE TEMPERATURES

Module case temperatures were recorded for three different cases.

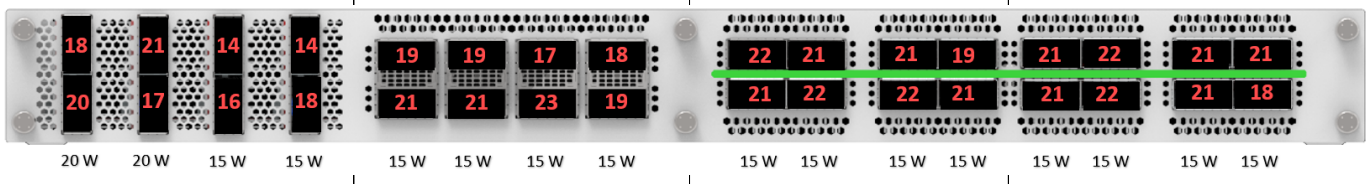
molex

Case 1 – Low Fan Speed

For case 1, fan duty cycle was set to 85% resulting in 206W power being consumed by the (8) fans. The airflow across each cage group at 85% duty cycle was measured using the wind tunnel.

Case 1

Fans	Delta T (°C)			
	1x2 QSFP-DD Vertical BiPass with Dual Heat Sinks	2x1 QSFP-DD Stacked	1x2 QSFP-DD Belly to Belly SMT	1x2 QSFP-DD Belly to Belly BiPass
Duty Cycly - 85% Power Consumed - 206 W	42 CFM	30 CFM	30 CFM	30 CFM

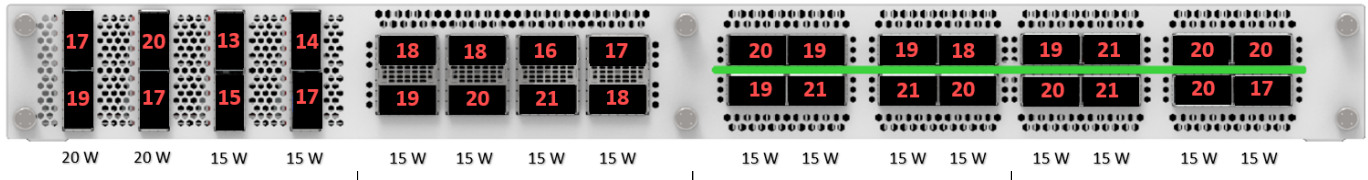


Case 2 – Medium Fan Speed

For case 2, fan duty cycle was set to 93% resulting in 224W power being consumed by the (8) fans. The airflow across each group at 93% duty cycle was measured using the wind tunnel.

Case 2

Fans	Delta T (°C)			
	1x2 QSFP-DD Vertical BiPass with Dual Heat Sinks	2x1 QSFP-DD Stacked	1x2 QSFP-DD Belly to Belly SMT	1x2 QSFP-DD Belly to Belly BiPass
Duty Cycly - 93% Power Consumed - 224 W	47 CFM	33 CFM	33 CFM	33 CFM

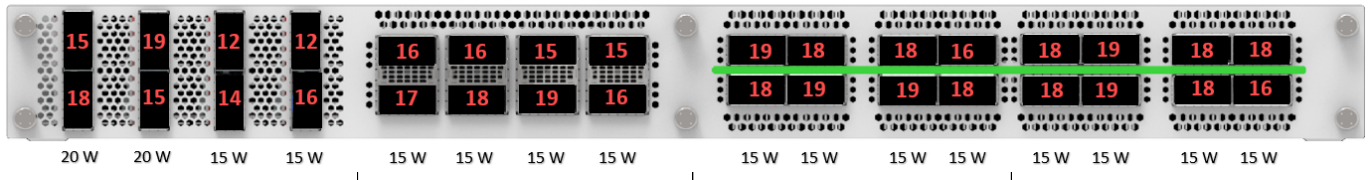


Case 3 – High Fan Speed

For case 3, fan duty cycle was set to 100% resulting in 242W power being consumed by the (8) fans. The airflow across each group at 100% duty cycle was measured using the wind tunnel.

Case 3

Fans	Delta T (°C)			
	1x2 QSFP-DD Vertical BiPass with Dual Heat Sinks	2x1 QSFP-DD Stacked	1x2 QSFP-DD Belly to Belly SMT	1x2 QSFP-DD Belly to Belly BiPass
Duty Cycly - 100% Power Consumed - 242 W	51 CFM	35 CFM	36 CFM	36 CFM



2.2 ASIC CORE TEMPERATURES

ASIC thermal loads were simulated to show that the ASIC can be cooled within specification at the respective power with preheat from 15W and 20W modules plugged in.

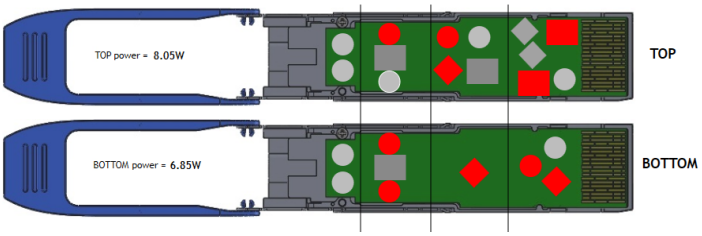
ASIC 1 (336W)	
Airflow (CFM)	Temperature (°C)
67	77
75	75
80	72

ASIC 2 (252W)	
Airflow (CFM)	Temperature (°C)
60	74
66	71
72	69

2.3 MODULE POWER

2.3.1 15W MODULES

Highlighted in red are the hotspots on the module, that were turned on to dissipate power, for the 15W power profile.



Hotspot Locations

The resistance values of the three different type of hotspots are shown below.

9 Ohms

6.75 Ohms

5.4 Ohms

Programmed Power Profile → $5\times\frac{3.3^2}{9}+3\times\frac{3.3^2}{6.75}+2\times\frac{3.3^2}{5.4}$ = **14.9W**

The Multilane modules were programmed to dissipate 14.9W when they receive 3.3V. Nevertheless, we decided to measure the actual voltage to determine the actual power dissipation (please note that the power dissipation equation is V2/R which implies that it's not as sensitive to the resistance). Using the measured voltage we were able to find the actual power dissipation by the modules. We have also included the fixed power dissipation from the microProcessor and the appropriate power dissipation from each MosFet.

Additional Power dissipated by the microProcessor and Mosfets = 0.558W (for 15W power profile)

THERMAL DEMO ACTUAL POWER DISSIPATION

1. **1x2 QSFP-DD Vertical BiPass with Dual Heat Sinks**

$$5\times\frac{3.229^2}{9}+3\times\frac{3.229^2}{6.75}+2\times\frac{3.229^2}{5.4}+0.558 = \mathbf{14.85W}$$

2. **2x1 QSFP-DD Stacked**
   Operating Voltage = 3.290V

$$5\times\frac{3.29^2}{9}+3\times\frac{3.29^2}{6.75}+2\times\frac{3.29^2}{5.4}+0.558 = \mathbf{15.39W}$$

3. **1x2 QSFP-DD Belly-to-Belly SMT**
   Operating Voltage = 3.288V

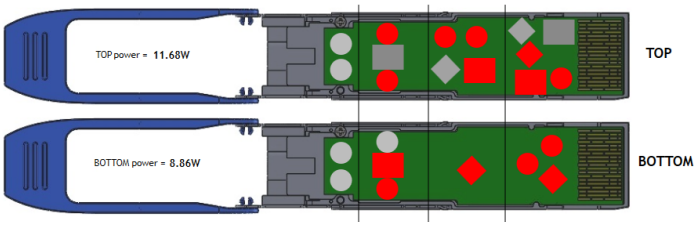
$$5\times\frac{3.288^2}{9}+3\times\frac{3.288^2}{6.75}+2\times\frac{3.288^2}{5.4}+0.558 = \mathbf{15.37W}$$

4. **1x2 QSFP-DD Belly-to-Belly BiPass**
   Operating Voltage = 3.290V

$$5\times\frac{3.29^2}{9}+3\times\frac{3.29^2}{6.75}+2\times\frac{3.29^2}{5.4}+0.558 = \mathbf{15.39W}$$

2.3.2 20W MODULE

Highlighted in red are the hotspots on the module, that were turned on to dissipate power, for the 20W power profile.



Hotspot Locations

Programmed Power Profile $\longrightarrow$ $8\times\frac{3.3^2}{9}+3\times\frac{3.3^2}{6.75}+3\times\frac{3.3^2}{5.4}$ **= 20.54W**

Four Multilane modules in the 1x2 QSFP-DD Vertical BiPass with Dual Heat Sinks cage group were programmed to dissipate 20.54W when they receive 3.3V. Nevertheless, we decided to measure the actual voltage to determine the actual power dissipation (please note that the power dissipation equation is V2/R which implies that it's not as sensitive to the resistance). Using the measured voltage we were able to find the actual power dissipation by the modules. We have also included the fixed power dissipation from the microProcessor and the appropriate power dissipation from each MosFet. For this power profile additional hotspots were turned on which resulted in relatively more power being dissipated by the Mosfets.

Additional power dissipated by microProcessor and Mosfets = 0.626W (for 20W power profile)

THERMAL DEMO ACTUAL POWER DISSIPATION

1. **1x2 QSFP-DD Vertical BiPass with Dual Heat Sinks**
   Operating Voltage = 3.229V

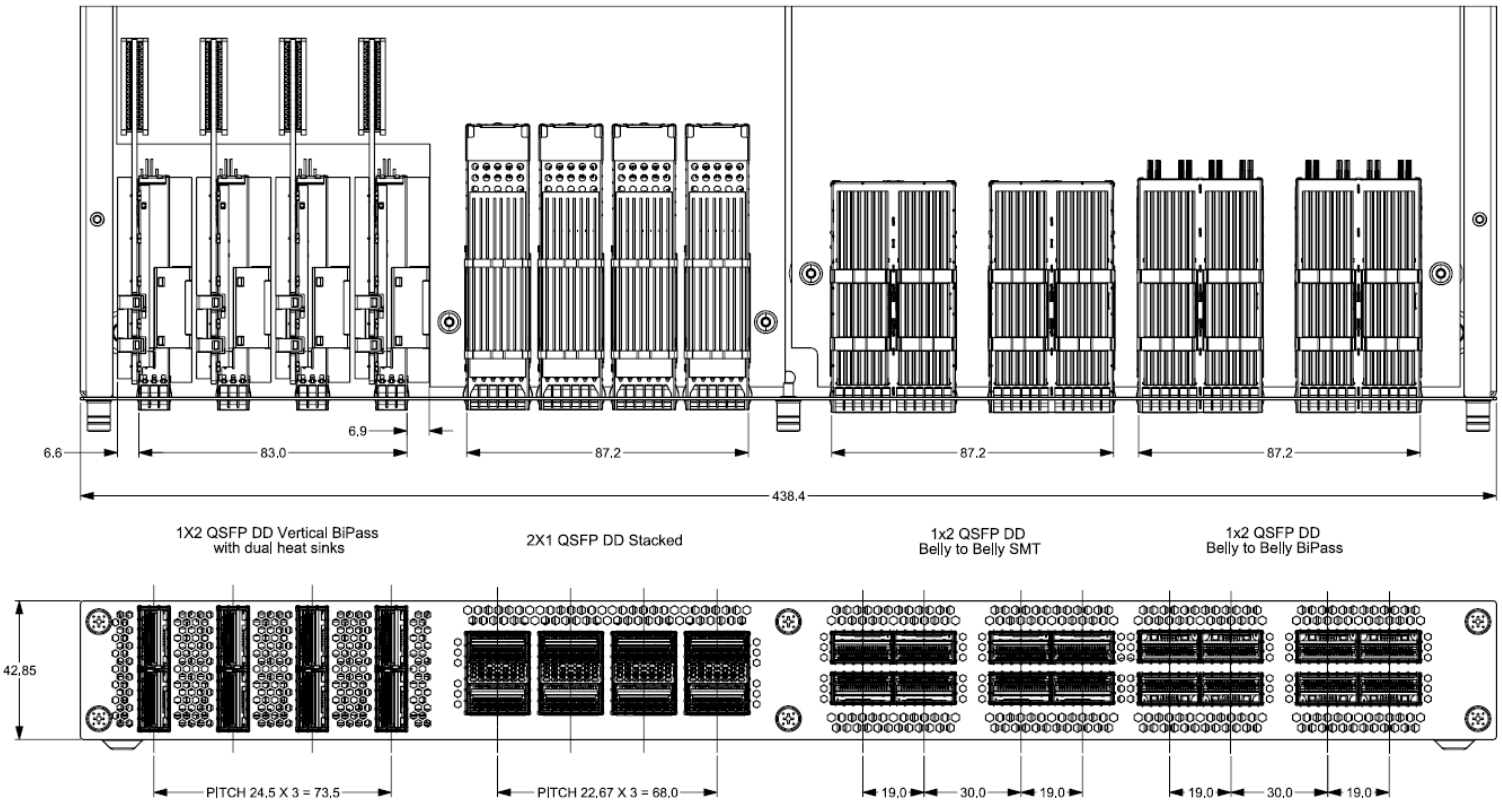
$$8\times\frac{3.229^2}{9}+3\times\frac{3.229^2}{6.75}+3\times\frac{3.229^2}{5.4}+0.626 = \mathbf{20.32W}$$

3. SYSTEM COMPONENTS

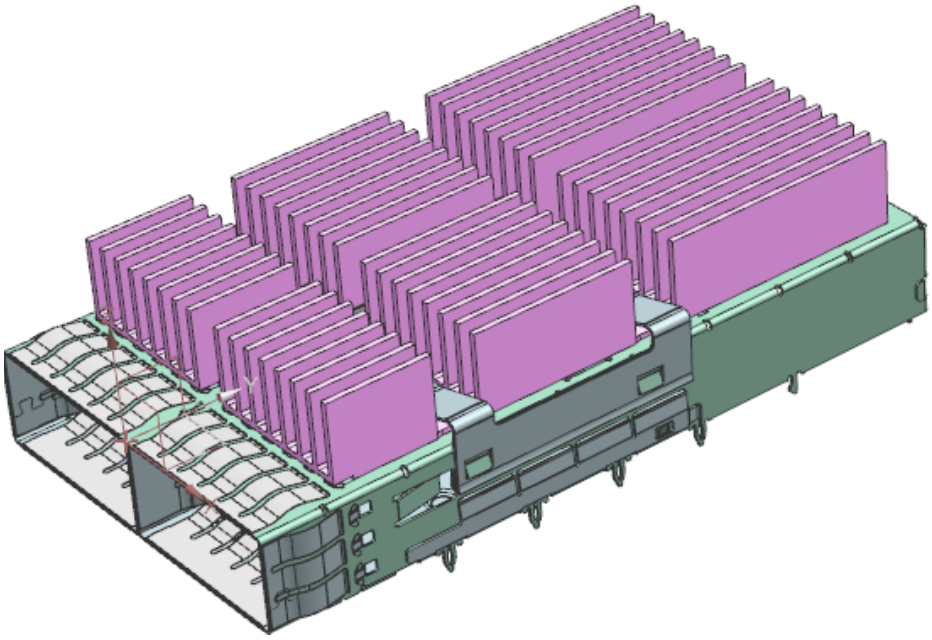
3.1 QSFP-DD CAGE TYPES

QSFP-DD Cage groups used in the thermal demo were divided into two main sub groups, cages mounted on mid-board and cages mounted on low-board.

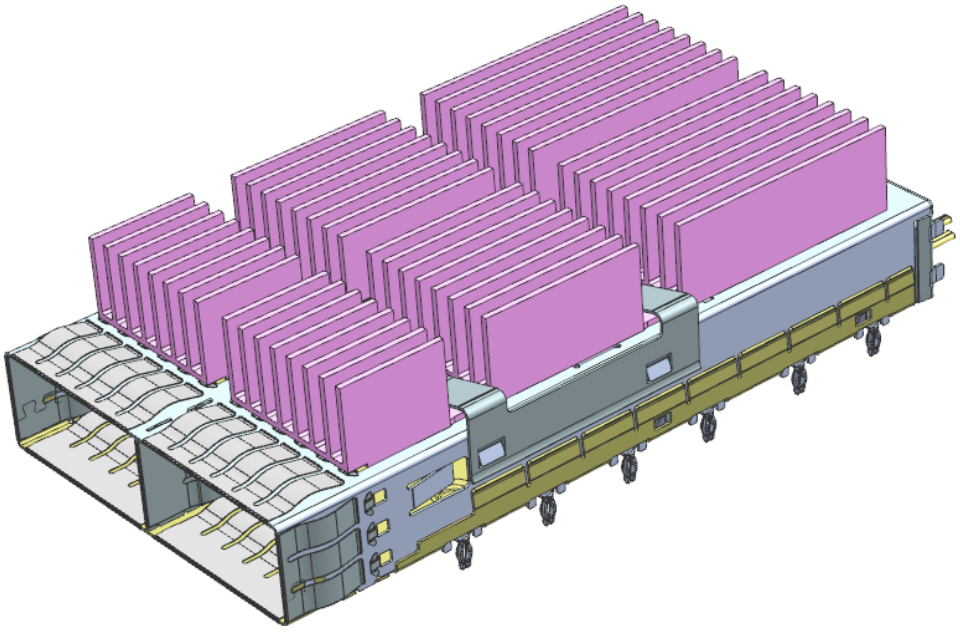
Pitch for the four different type of cage groups is shown below.



3.11 MID-BOARD

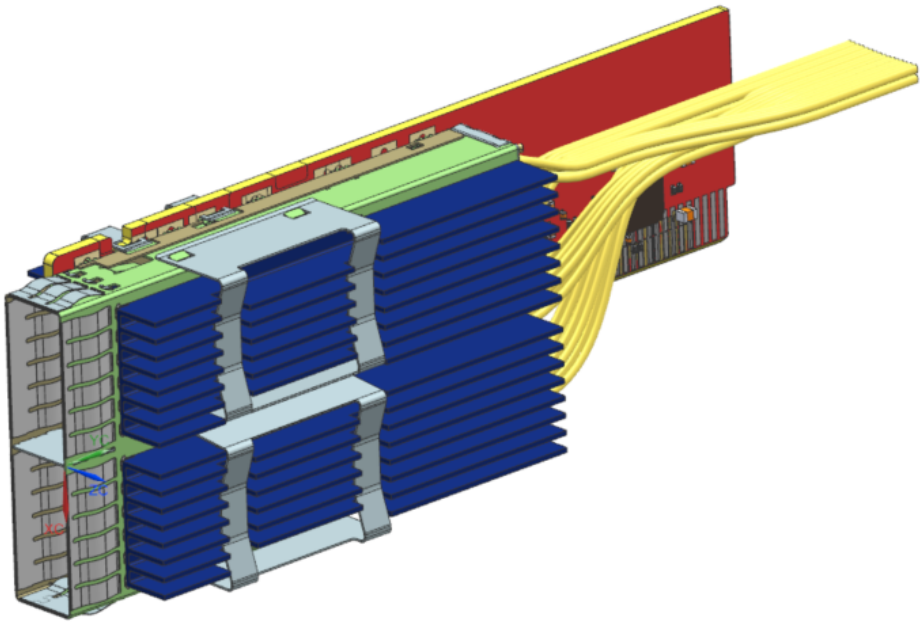


1x2 QSFP-DD Belly-to-Belly SMT (Molex P/N: 2031521350)

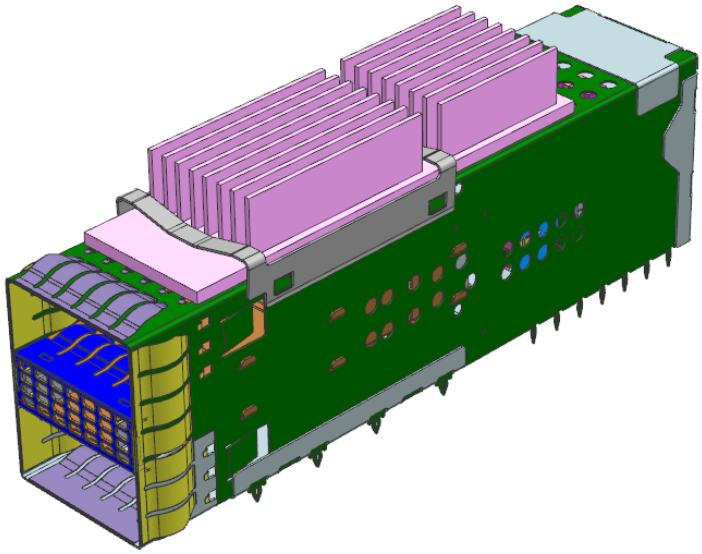


1x2 QSFP-DD Belly-to-Belly BiPass (Molex P/N: 2063582004 and 2063582504)

3.12 LOW-BOARD



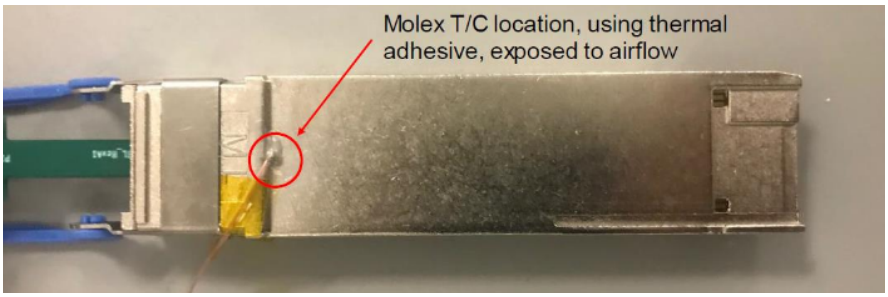
1x2 QSFP-DD Vertical BiPass with Dual Heatsinks (Molex P/N: 2009983050)



2x1 QSFP-DD Stacked (Molex P/N: 2040586101)

3.2 MODULES

32 Multilane ML 4062-S-TL1-LCD were used. Module LCDs were calibrated to show the temperature delta at the location shown below.



LCD reading calibrated to show the temperature delta at the location shown

Modules in thermal demo recorded the temperature at Temp Sense 2 positioned on the shell (location shown below). To calibrate this reading such that the LCD screens show the temperature delta at the Molex thermocouple location additional thermal testing was done to determine a correction factor. This correction factor was subtracted from the reading at Temp Sense 2. LCD screen temperature delta was determined using the following equation:

(LCD Temperature Delta) = (Temperature at Temp Sense 2) – (Ambient Temperature) – (Correction Factor)

Module temperature sensor location

Correction factors for each group are shown below.

	1x2 QSFP-DD Vertical BiPass with Dual Heat Sinks (20 W)	1x2 QSFP-DD Vertical BiPass with Dual Heat Sinks (15 W)	2x1 QSFP-DD Stacked (Top)	2x1 QSFP-DD Stacked (Bottom)	1x2 QSFP-DD Belly-to-Belly SMT	1x2 QSFP-DD Belly-to-Belly BiPass
Correction Factor (°C)	13.8	9.6	14.4	16.8	16.7	16.6

3.3 ASIC

21.5W @ 12V DC Watlow Ceramic heaters were used to simulate the heat generated by the ASIC. On the left side (low board) 16 heaters were turned on resulting in 336W. On the right side (mid board) 12 heaters were turned on resulting in 252W.

3.4 FANS

8 (4 for low board and 4 for mid board) Sanyo Denki America Inc. 9CRH0412P5J001 were used in the thermal demo.

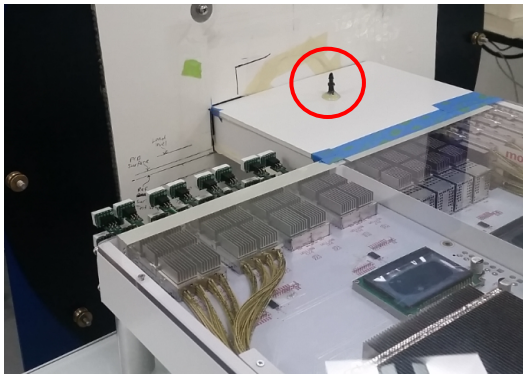
3.5 I2C COMMUNICATION FOR TEMPERATURES

All the temperatures in the thermal demo were recorded using I2C communication. 32 Multilane modules plugged in the thermal demo have an I2C channel that transfers temperature data recorded by the temperature sensor in the MultiLane thermal module to the 7-segment display plugged into the 6-pin header in the front of the MultiLane thermal module, as well as the Raspberry Pie. The 32 I2C channels communicate with the Raspberry Pie via four - 8 channel I2C switches. Temperatures at the two ASICs and the ambient temperature are measured using thermocouples, which then transfer this temperature information to the Raspberry pie using I2C channels. The Raspberry pie then processes this information to be

displayed on the GUI as well as the LCD screens soldered onto the motherboards that show the ASIC temperature.

4. SYSTEM AIRFLOW MEASUREMENT

Setup to measure airflow across each cage group is shown below. To measure the airflow, the pressure at the nozzle highlighted in red was made equal to the ambient pressure for each fan duty cycle by adjusting the wind tunnel airflow. The resulting airflow at equilibrium (pressure) was recorded.



Setup for Airflow measurement

Airflow for 1x2 QSFP-DD Vertical BiPass with Dual Heatsinks cage group was observed to be significantly higher. This is mainly due to the opening surface area. 1x2 QSFP-DD Vertical BiPass with Dual Heatsinks cage group has an opening surface area of 831mm^2, compared to 2x1 QSFP-DD Stacked cage group which has an opening surface area of 551mm^2. 1x2 QSFP-DD Belly-to-Belly SMT and 1x2 QSFP-DD Belly-to-Belly BiPass, both have an opening surface area of 540mm^2 due to which they have the same airflow across them. This applies for Case 2 and Case 3 as well.

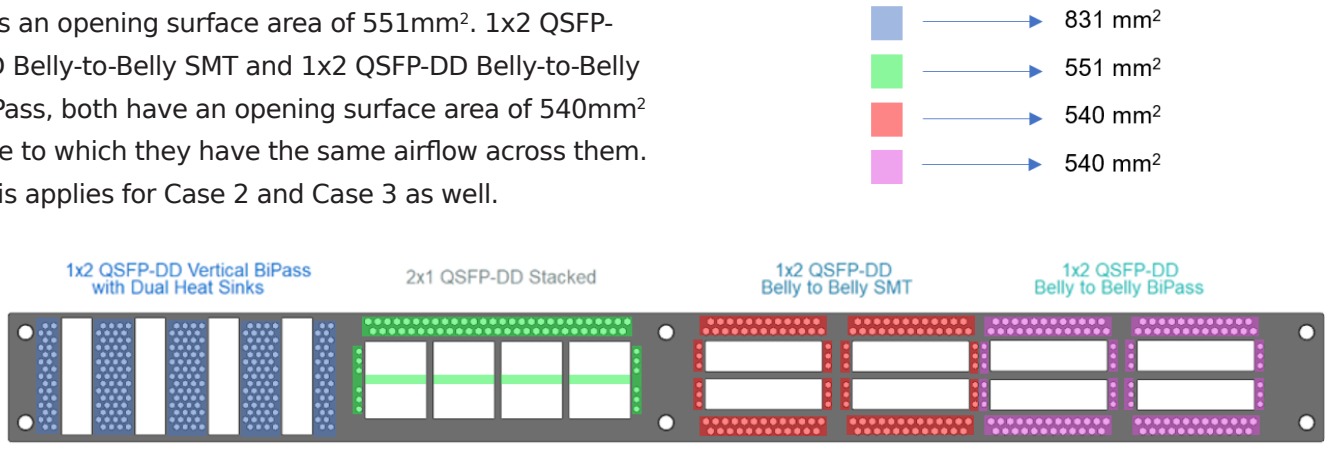
Opening surface area for each cage group was found by calculating the surface area of the vent holes around each group as highlighted below (opening surface area for 2x1 QSFP-DD Stacked cage group also includes the open area between the top and bottom port).

5. CONCLUSION

Molex cage products were able to cool the QSFP-DD modules to within specification. 1x2 QSFP-DD Vertical BiPass with Dual Heat Sinks cage group was able to cool even the modules dissipating 20W to within specification.

The Multilane modules used in the Thermal Demo can be programmed to different power profiles based on the requirement.

Molex Thermal Demo for DesignCon is available for demonstration upon request.



Thermal Demo Front Panel

Order No. 987652-0791 USA/0K/GF/2019.07