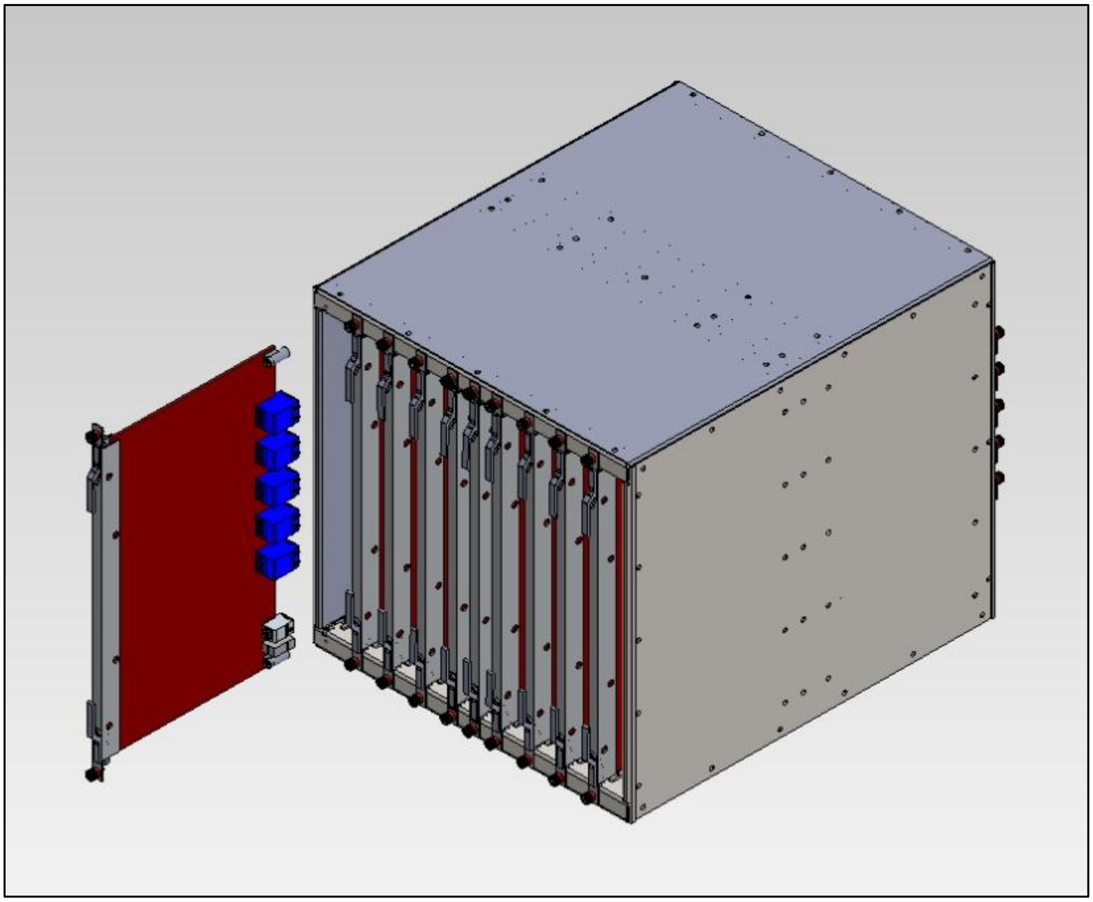
molex IMPACT

REFERENCE DESIGN

ORTHOGONAL DIRECT SYSTEM TOLERANCE COMPARISON ANALYSIS

REVISION	DESCRIPTION	INITIAL	DATE
01	Initial release	PAH	3/19/2012



Montie Design
www.montie.com

BACKGROUND

This report is a follow-on document to the original paper “Impact Orthogonal Direct System Tolerance Analysis, Revision: 1”. For an explanation of the tolerance analysis methodology and description of terms please refer to that paper first. (See Appendix A)

This paper answers the following question: “How does the OD connector system compare in tolerance stack up to traditional midplane systems with regards to mating boards and connectors; will connectors mate without crashing and will there be enough engagement for adequate pin wipe?” To answer this question also requires addressing the question: “What is the typical dimensional loop for computing tolerance stack up?” A card cage reference design is provided by Montie Design. Tolerance loops are created from this design. Analysis of the tolerance loops will measure the probability of achieving a working assembly. By demonstrating several different tolerance loops that exist in the reference chassis design you will learn how to apply these techniques to your specific design. Knowing where the construction choices affect the tolerance build up will allow you to consider different construction techniques to improve your design.

REFERENCE DESIGN

The card cage is a sheet metal assembly. The cage is riveted together. Proper alignment is controlled by identifying a single locating point for mating pieces; all features are controlled and measured from this locating hole. Tolerances build up as dimensions from one feature to the next string together to define the assembly process.

The reference design addresses the construction for supporting the IO, Management, and Fabric cards only. A complete design will also include air flow and power supply considerations. These elements have not been included in the reference design, but a few design options will be discussed.

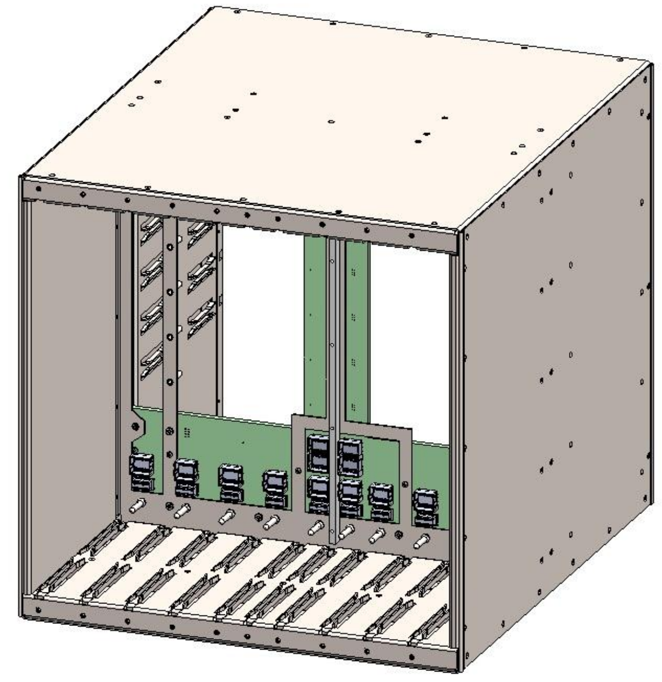


Figure 1 Reference Card Cage

The OD design adds an air flow design option which allows direct flow from front to back. The midplane can be completely open around the IO to

Fabric board connections. Traditional designs must create air flow paths that are separate for the front and rear cards.

How the card cage is assembled plays an important role in the dimensional loops. This design rivets the panels together, though welding or other fasteners can also be used. Typical construction uses aligning holes and may use jigs and fixtures to support and locate panels as they are assembled. This is a further means of controlling the total tolerance build up in the design.

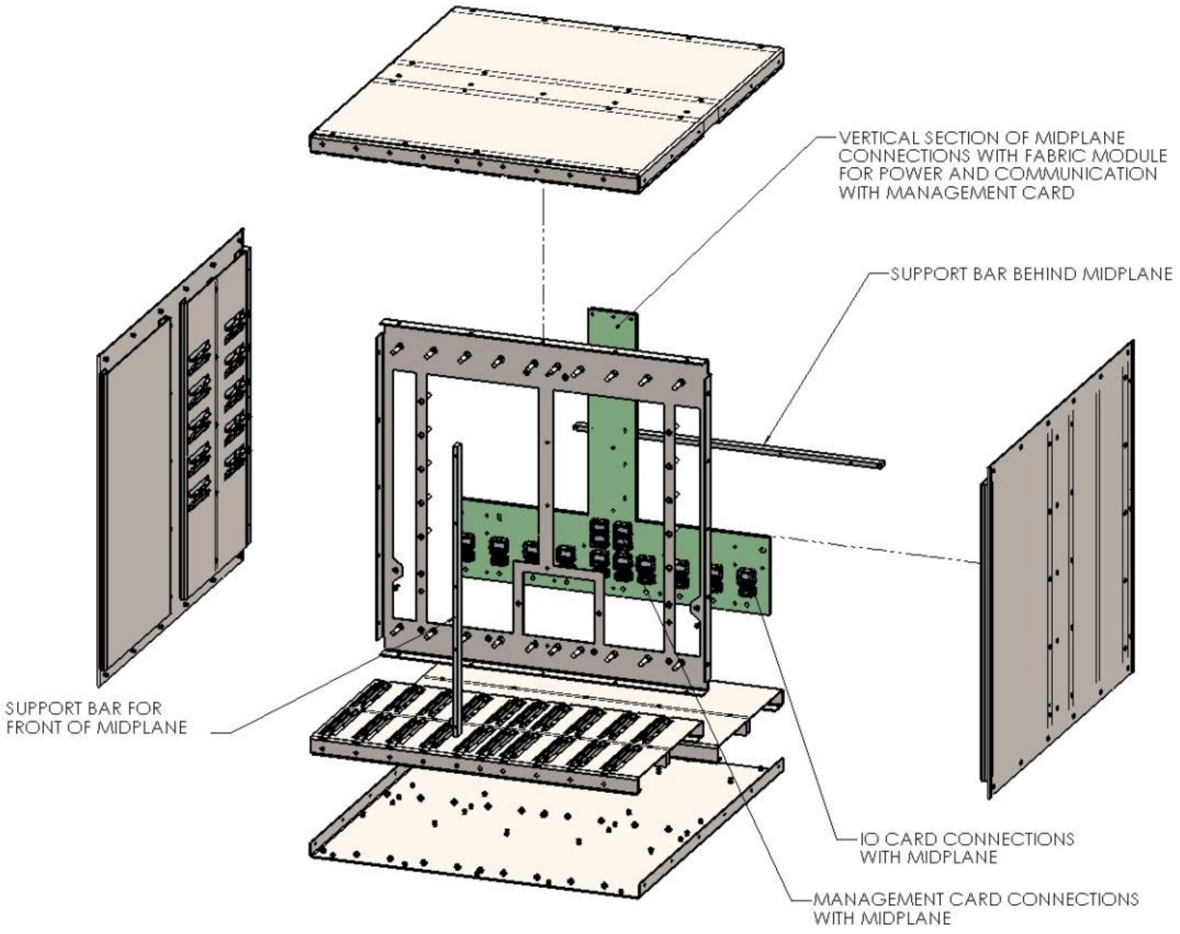


Figure 2: Card Cage, exploded view

Figure 2 shows an exploded view of the reference design. The midplane is constructed in the shape of an upside down T. Connectors on the lower section of the midplane provide communication between the Management and the IO cards. The midplane also provides power connectors to the Management and IO cards. The vertical section of the midplane is used to provide power connection to the Fabric cards. It also provides communication signals between the Management and Fabric cards in this reference design. The designer does have the option to use OD connectors for communication between the Management and Fabric cards. The vertical section of the midplane could potentially be eliminated if power can be supplied to the Fabric cards via an alternate path (i.e. separate card or power buss.) In this

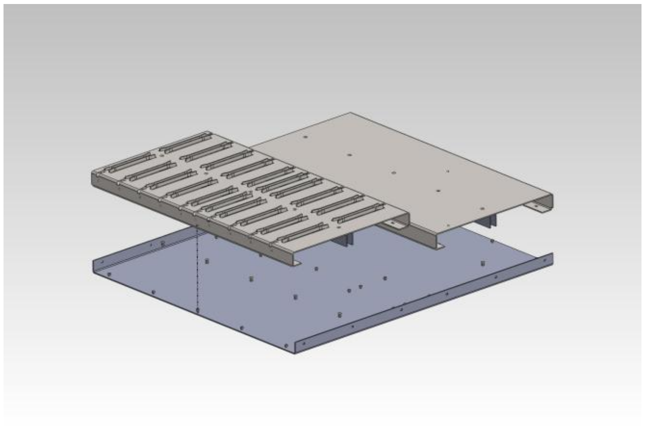


Figure 4: Bottom Panel subassembly, exploded view

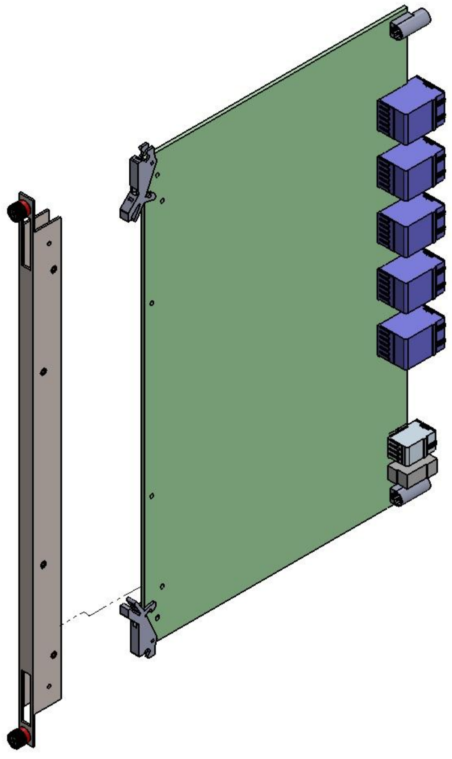


Figure 3: Card Assembly, face plate attachment

reference design you will also see two stiffener bars, one on each side of the midplane. These provide support against the insertion forces as cards are inserted into the midplane and also prevent the boards from bowing.

The midplane panel is the starting point for construction. Locating holes are used to align subassemblies as they are attached. Critical features of each part are controlled with respect to the locating hole. The purpose is to reduce the number of stacked tolerances. To locate each of the panel subassemblies to the midplane panel, only one of the rivet holes is a round hole, the rest are elongated to allow for tolerance variability. When the rivet is attached through this locating hole, the compression will take up all clearances and pull the two panels into position. Therefore, each side panel (Top, Bottom, Right and Left) is assembled to the midplane panel in controlled position. Subassemblies follow the same construction pattern. One rivet hole is the locating feature. Figure 3 shows how the edge guide panel is riveted to the bottom panel to build up this subassembly. Tracing the dimension loop from feature to feature through the controlled locating holes gives the tolerance loop. Controlling dimensions to the reference locating holes reduces the number of dimensions and tolerances that need to be considered.

The card assemblies follow the same methodology. For each attached feature that is critical to the locating function, a reference locating hole and mating pin joins the components together.

TOLERANCE LOOP CONSTRUCTION

The basic technique is to choose the connector interface to study and to find the nominal gap that is built into the design. Then create a loop of the defining dimensions that run from one face all the way around the assembly and back to the opposite mating face. There are two sequences of mating components as the boards come together. First is the initial mating of a guide pin into the mating barrel receptacle. Second is the mating of the signal or power connectors. Each mating pair contains a designed nominal clearance or gap to allow for tolerance variations so the parts can be assembled without “crashing”. The tolerance stack up results in a statistical probability around how much this gap shrinks to the point where if it becomes negative we will have an interference and failure of the components to slide together.

Directions will be defined as follows.

X = left to right when looking at the front of the chassis,
Y = bottom to top,
Z = front to back.

CONNECTOR PIN ENGAGEMENT

The first tolerance study is in the Z direction, the seating of the connectors. There are two design approaches. One is to design the cards to be inserted fully until the first connector bottoms out against the mating connector on the midplane or the orthogonal pair. Designing the nominal gap to be zero means the tolerance loop will predict interference for half of the cards. This interference will exhibit itself somewhere else in the design. For example, in the reference chassis, this would show up as a gap between the card face plate and the front edge of the chassis edge guide panel. It is up to the designer to determine the criterion and create a design that meets these needs.

The other design approach is to design in an intentional gap between the connectors as the nominal design condition. A larger gap lowers the probability of an interference. If the gap is too generous though, the tolerance spread in the opposite direction would result in the connectors failing to mate sufficiently. The designer needs to determine if there is enough pin length engagement left in the connection to ensure that the electrical contact will be reliable. The designer sets the minimum amount of pin wipe allowed for the design and compares this to the amount that exists in the worst case tolerance build up expected. The reference design is based on this second approach.

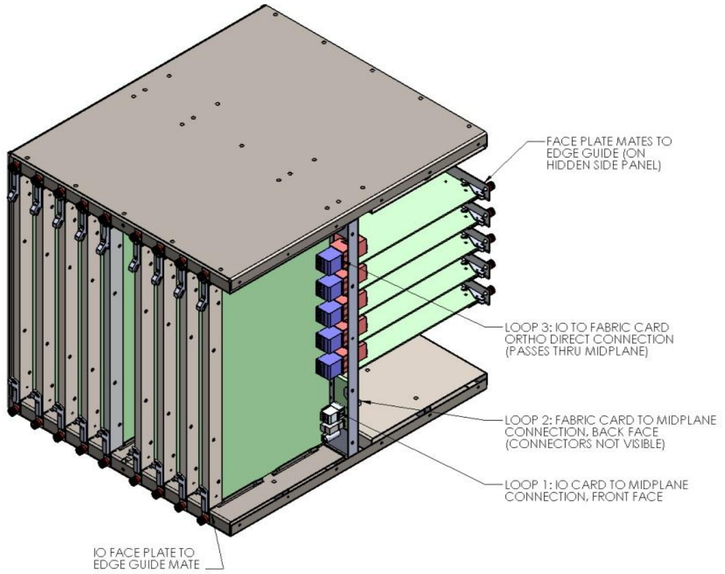


Figure 5: Z Loop Definitions, connector engagement

So to reiterate these design points:

1. The signal characteristics for high-speed transmissions need to be understood and included in the

mechanical design considerations.
2. Fully seated vs. partially seated connectors and a means to secure the card to restrict movement after insertion in the cage are inter-related design considerations.

We have three dimensional loops to consider.

1. IO cards as they mate with the connectors on the midplane.
2. Fabric cards as they mate to the back side of the midplane.
3. The orthogonal connection of the IO to the Fabric cards.

In a traditional design, dimensional Loops 1 and 2 are already a common occurrence. This provides a baseline for comparisons between the reference design in this paper and the reader's particular design. The user can compare construction techniques and tolerance parameters with his/her typical construction and compare the computations for tolerance stack ups.

Loop 3 is unique to the OD connection system. The following analysis shows the tolerance variations are comparable to 1 and 2, generally falling between the two ranges.

LOOP 1

The first Loop study will be the mating of the IO card to the Midplane. Initially the design assumes zero nominal gap between the mating connectors on the IO Card and the Midplane. The results can be used to see the effect of different designed gaps on the probability of interference. Figure 6 shows the relevant dimensions of the IO card assembly for the tolerance loop.

D1 = connector dimension from the mating face to the location of P1. Since the pins are a press fit into the board, there are no hole clearance dimensions included.

D2 = P1 location to the reference locating hole for the PCB to the Face Plate. In this case the assembly could be a clearance fit around the pin to hole in the face plate. This clearance is included as an added tolerance.

D3 = distance from the locating hole on the face plate to the locating surface of the face plate that is screwed against the front of the edge guide panel.

The dimensional loop now moves to the Edge Guide panel subassembly.

D4 = distance from front folded edge to the locating reference hole that attaches to the top panel. Assume all clearance is taken up by the rivet, so no tolerance is necessary for the clearance.

D5 = distance from the edge guides' locating hole in the top panel to the locating hole for the midplane panel. Again, no clearance will be left after the rivet is clinched.

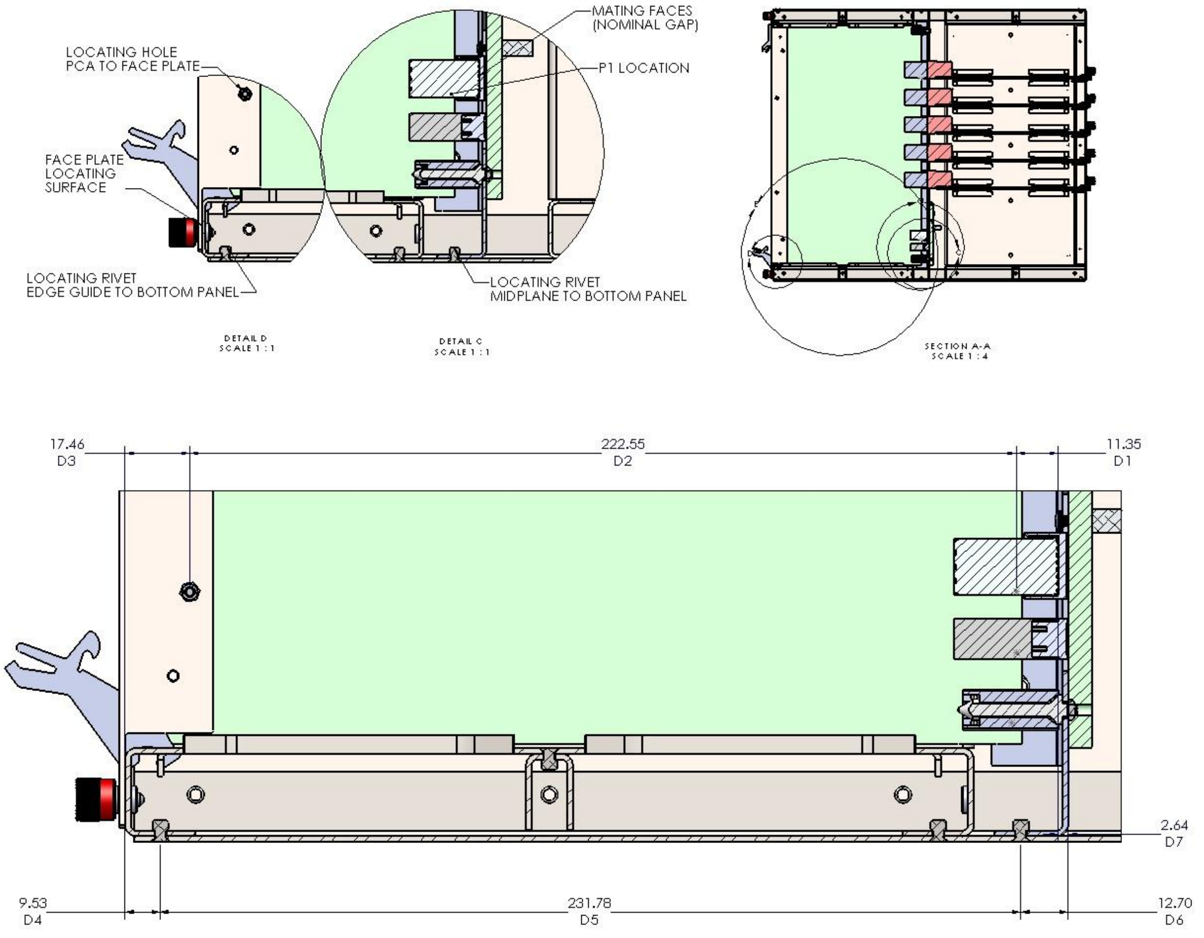


Figure 6: LOOP 1 Dimensions

Next we traverse to the midplane panel subassembly, including the midplane PCB.

D6 = distance from the locating hole on the top bend of the midplane panel to the face of the midplane panel. The Midplane PCB will be secured against this face so it is the reference surface.

D7 = the dimension of the mating connector, from the surface against the PCB to the mating face inside the connector. There will be a dimensional tolerance. Also, there will be a tolerance for the variability that represents the connector not fully seated against the board.

For a better view of the locating dimensions on the bottom panel, see Figure 7.

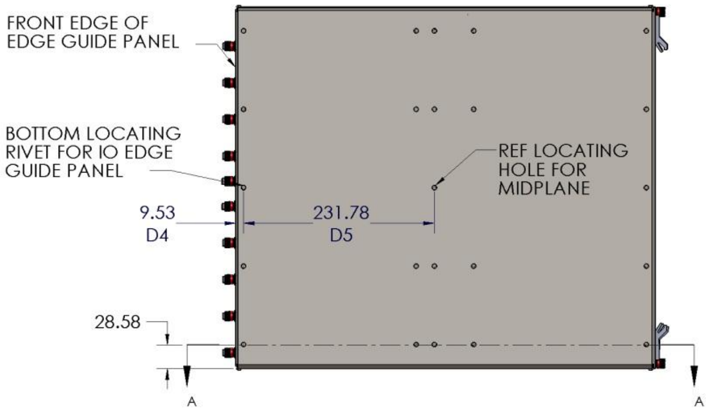
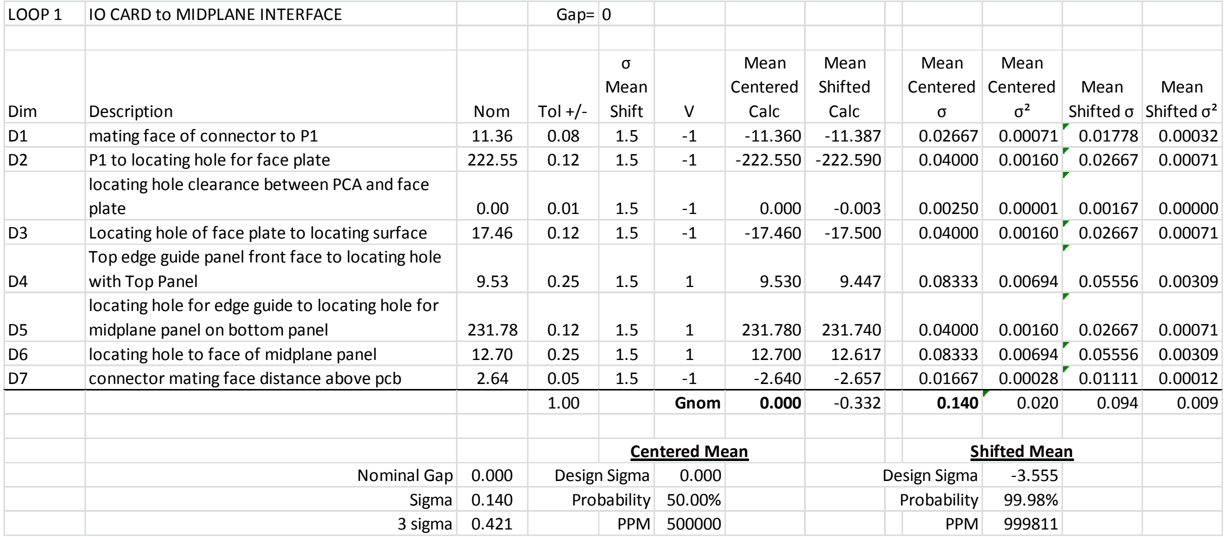


Figure 7: Loop 1 Bottom panel dimensions

That completes the loop. Tables 1-3 show the computation results. Look at the calculations to see how the tolerances stack up and to see where to set the nominal gap.

In the first calculation with a designed gap of zero, the computed tolerance sigma is 0.14mm. A good computation point would thus be a nominal gap of 0.5mm. The nominal gap should also be chosen by looking at the total pin wipe available. Impact connectors will have up to 2mm of wipe, so a nominal gap of 0.5mm is still a reasonable design point.

Table 1: LOOP 1, no gap



LOOP 1	IO CARD to MIDPLANE INTERFACE		Gap=	0							
Dim	Description	Nom	Tol +/-	σ Mean Shift	V	Mean Centered Calc	Mean Shifted Calc	Mean Centered σ	Mean Centered σ²	Mean Shifted σ	Mean Shifted σ²
D1	mating face of connector to P1	11.36	0.08	1.5	-1	-11.360	-11.387	0.02667	0.00071	0.01778	0.00032
D2	P1 to locating hole for face plate	222.55	0.12	1.5	-1	-222.550	-222.590	0.04000	0.00160	0.02667	0.00071
	locating hole clearance between PCA and face plate	0.00	0.01	1.5	-1	0.000	-0.003	0.00250	0.00001	0.00167	0.00000
D3	Locating hole of face plate to locating surface	17.46	0.12	1.5	-1	-17.460	-17.500	0.04000	0.00160	0.02667	0.00071
D4	Top edge guide panel front face to locating hole with Top Panel	9.53	0.25	1.5	1	9.530	9.447	0.08333	0.00694	0.05556	0.00309
D5	locating hole for edge guide to locating hole for midplane panel on bottom panel	231.78	0.12	1.5	1	231.780	231.740	0.04000	0.00160	0.02667	0.00071
D6	locating hole to face of midplane panel	12.70	0.25	1.5	1	12.700	12.617	0.08333	0.00694	0.05556	0.00309
D7	connector mating face distance above pcb	2.64	0.05	1.5	-1	-2.640	-2.657	0.01667	0.00028	0.01111	0.00012
			1.00		**Gnom**	**0.000**	-0.332	**0.140**	0.020	0.094	0.009
				Centered Mean				**Shifted Mean**			
	Nominal Gap	0.000		Design Sigma	0.000			Design Sigma	-3.555		
	Sigma	0.140		Probability	50.00%			Probability	99.98%		
	3 sigma	0.421		PPM	500000			PPM	999811		

If you look at the probability of interference, you see the calculation is 50%. This is because the nominal gap is zero. Half of the time the tolerances will be greater than zero; half of the time less than zero. Open the gap to get the probability or parts per million (PPM) down to an acceptable number.

Tables 2 and 3 show the computations if the design included a nominal gap of 0.5 and 1.0mm by making the PCB shorter (D2). Look at the results for the probability of interference.

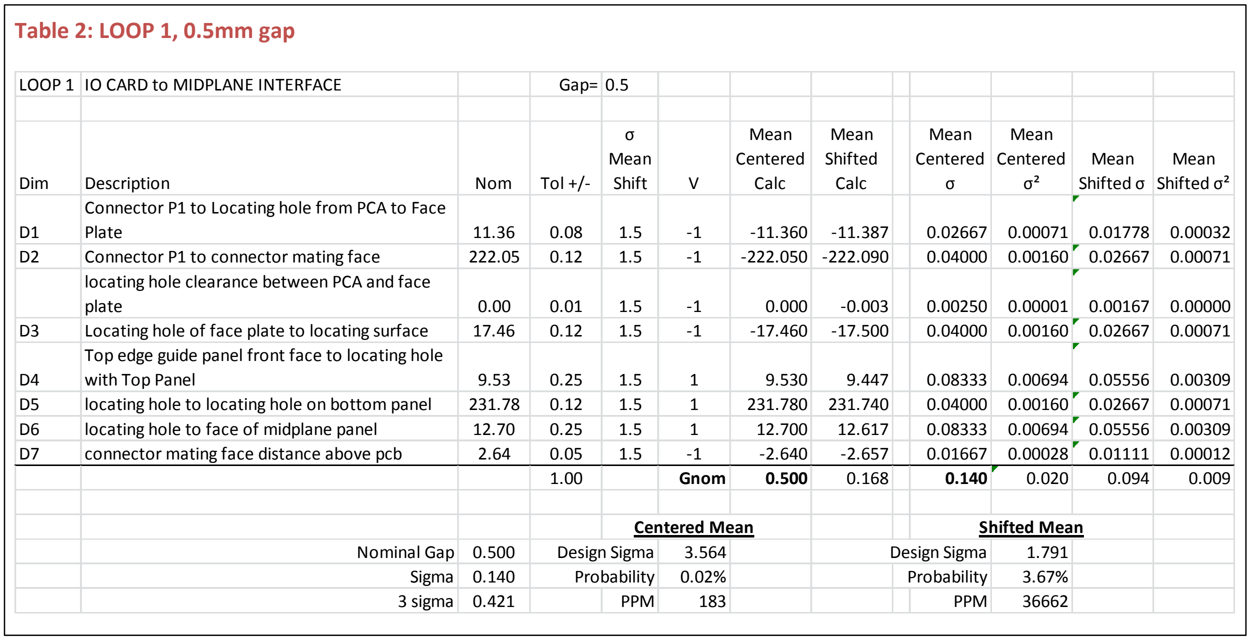


Table 2: LOOP 1, 0.5mm gap

LOOP 1	IO CARD to MIDPLANE INTERFACE		Gap=	0.5							
Dim	Description	Nom	Tol +/-	σ Mean Shift	V	Mean Centered Calc	Mean Shifted Calc	Mean Centered σ	Mean Centered σ²	Mean Shifted σ	Mean Shifted σ²
D1	Connector P1 to Locating hole from PCA to Face Plate	11.36	0.08	1.5	-1	-11.360	-11.387	0.02667	0.00071	0.01778	0.00032
D2	Connector P1 to connector mating face	222.05	0.12	1.5	-1	-222.050	-222.090	0.04000	0.00160	0.02667	0.00071
	locating hole clearance between PCA and face plate	0.00	0.01	1.5	-1	0.000	-0.003	0.00250	0.00001	0.00167	0.00000
D3	Locating hole of face plate to locating surface	17.46	0.12	1.5	-1	-17.460	-17.500	0.04000	0.00160	0.02667	0.00071
D4	Top edge guide panel front face to locating hole with Top Panel	9.53	0.25	1.5	1	9.530	9.447	0.08333	0.00694	0.05556	0.00309
D5	locating hole to locating hole on bottom panel	231.78	0.12	1.5	1	231.780	231.740	0.04000	0.00160	0.02667	0.00071
D6	locating hole to face of midplane panel	12.70	0.25	1.5	1	12.700	12.617	0.08333	0.00694	0.05556	0.00309
D7	connector mating face distance above pcb	2.64	0.05	1.5	-1	-2.640	-2.657	0.01667	0.00028	0.01111	0.00012
			1.00		**Gnom**	**0.500**	0.168	**0.140**	0.020	0.094	0.009
					Centered Mean				**Shifted Mean**		
	Nominal Gap	0.500		Design Sigma	3.564			Design Sigma	1.791		
	Sigma	0.140		Probability	0.02%			Probability	3.67%		
	3 sigma	0.421		PPM	183			PPM	36662		

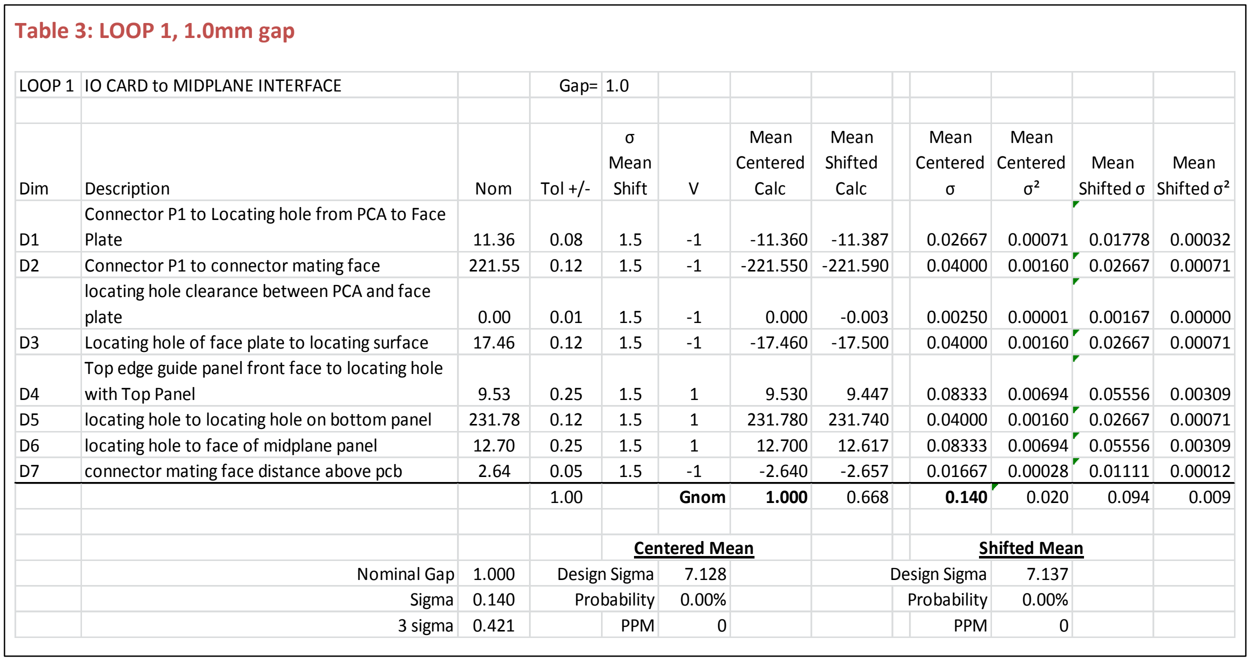


Table 3: LOOP 1, 1.0mm gap

LOOP 1	IO CARD to MIDPLANE INTERFACE		Gap=	1.0							
Dim	Description	Nom	Tol +/-	σ Mean Shift	V	Mean Centered Calc	Mean Shifted Calc	Mean Centered σ	Mean Centered σ²	Mean Shifted σ	Mean Shifted σ²
D1	Connector P1 to Locating hole from PCA to Face Plate	11.36	0.08	1.5	-1	-11.360	-11.387	0.02667	0.00071	0.01778	0.00032
D2	Connector P1 to connector mating face	221.55	0.12	1.5	-1	-221.550	-221.590	0.04000	0.00160	0.02667	0.00071
	locating hole clearance between PCA and face plate	0.00	0.01	1.5	-1	0.000	-0.003	0.00250	0.00001	0.00167	0.00000
D3	Locating hole of face plate to locating surface	17.46	0.12	1.5	-1	-17.460	-17.500	0.04000	0.00160	0.02667	0.00071
D4	Top edge guide panel front face to locating hole with Top Panel	9.53	0.25	1.5	1	9.530	9.447	0.08333	0.00694	0.05556	0.00309
D5	locating hole to locating hole on bottom panel	231.78	0.12	1.5	1	231.780	231.740	0.04000	0.00160	0.02667	0.00071
D6	locating hole to face of midplane panel	12.70	0.25	1.5	1	12.700	12.617	0.08333	0.00694	0.05556	0.00309
D7	connector mating face distance above pcb	2.64	0.05	1.5	-1	-2.640	-2.657	0.01667	0.00028	0.01111	0.00012
			1.00		**Gnom**	**1.000**	0.668	**0.140**	0.020	0.094	0.009
					Centered Mean				**Shifted Mean**		
	Nominal Gap	1.000		Design Sigma	7.128			Design Sigma	7.137		
	Sigma	0.140		Probability	0.00%			Probability	0.00%		
	3 sigma	0.421		PPM	0			PPM	0		

With a 0.5mm nominal gap, the probability of interference (bottoming out) is down to 0.02% (183PPM); at a 1.0mm nominal gap, the probability shrinks to essentially zero. What about too much gap?

At the other end of the tolerance stack up, the question is whether there will be enough pin engagement for a reliable connection. For example, using the 5.5mm pin length Impact connectors provides a maximum pin wipe of 2.0mm. At the maximum probable gap (nominal gap plus 3 sigma) the minimum amount of pin wipe will be the total pin wipe minus the nominal gap minus 3 times the tolerance standard deviation (3 sigma). For 0.5mm nominal gap the computed minimum pin wipe is 2-0.5-0.421= 1.079mm. For 1.0mm nominal gap the minimum pin wipe is only 0.579mm Using this approach, a designed nominal gap of 1mm will not provide the desired pin engagement.

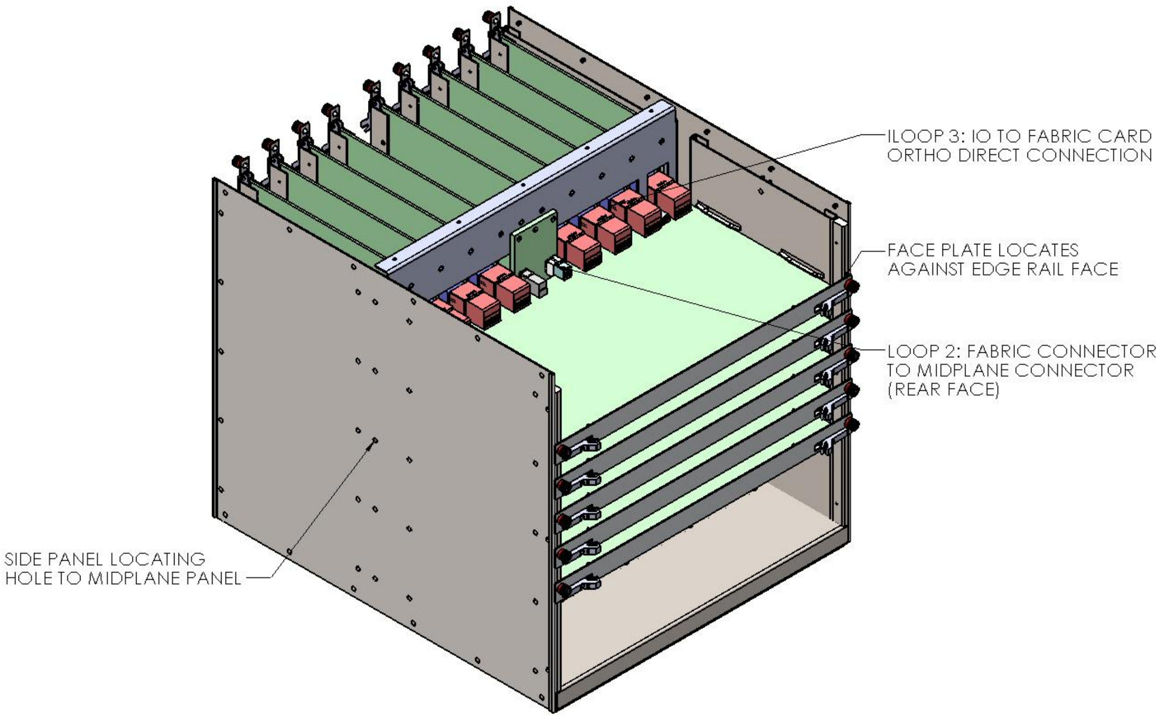


Figure 8: Loop 2 configuration

LOOP 2

Loop 2 is similar to Loop 1, but adds in the midplane board thickness. In this loop, the mating connector is on the back side of the Midplane PCB; the dimension loop for the midplane goes from top face of the PCB to the back side (board thickness). The mating connector is on the back side of the PCB. Loop 2 consists of all the dimensions in Loop 1 plus one added dimension of the midplane PCB thickness. Actual dimensions will vary depending on the design of the fabric card sizes and depth of the card cage, but the associated tolerances will be similar. You will note that in this loop, the manufacturing tolerance of the board thickness is a significant component of the total tolerance, and is much larger than any other dimensional tolerance. The card thickness tolerance is typically +/- 10% so the thicker the board, the larger the tolerance. The reference design assumes a 6.45mm thick midplane. A thicker board provides more stiffness and layers for routing signals. A thinner board will have less tolerance, so the designers need to balance these factors in selecting the design thickness of the midplane. Generally, the electrical characteristics will take precedence over mechanical properties.

Beginning at the Fabric card connector:

> R1 = connector dimension from the mating face to the location of P1. Since the pins are a press fit into the board, we don't need to include any hole clearance in the study.
>
> R2 = P1 location to the reference locating hole for the PCB to the Face Plate. In this case the assembly could be a clearance fit around the pin to hole in the face plate. We need to include this clearance as an added tolerance.
>
> R3 = distance from the locating hole on the face plate to the locating surface of the face plate that is screwed against the front of the edge guide panel. The face plate is screwed fast against the edge rail, so there will be no clearance.

Next move to the Side Panel dimensions:

> R4 = distance from front face of edge rail to the locating reference hole that attaches the rail to the side panel. We assume that the counter sink head will hold the parts in location, so the tolerance is not for clearance, but is for concentricity of screw head to shank.
>
> R5 = distance from the edge guide's locating hole in the side panel to the locating hole for the midplane panel. Again no clearance will be left after the rivet is clinched

End with the Midplane panel and the Midplane PCB.

> R6 = distance from the locating hole on the side bend of the midplane panel to the face of the midplane panel. The Midplane PCB will be secured against this face so it is the reference surface.
>
> R7 = the dimension of the mating connector, from the surface against the PCB to the mating face inside the connector. There will be a dimensional tolerance. Also, there will be a tolerance for the variability that represents the connector not fully seated against the board.
>
> R8 = thickness of midplane PCB. In the loop, R8 comes before R7. For computation purposes this doesn't matter.

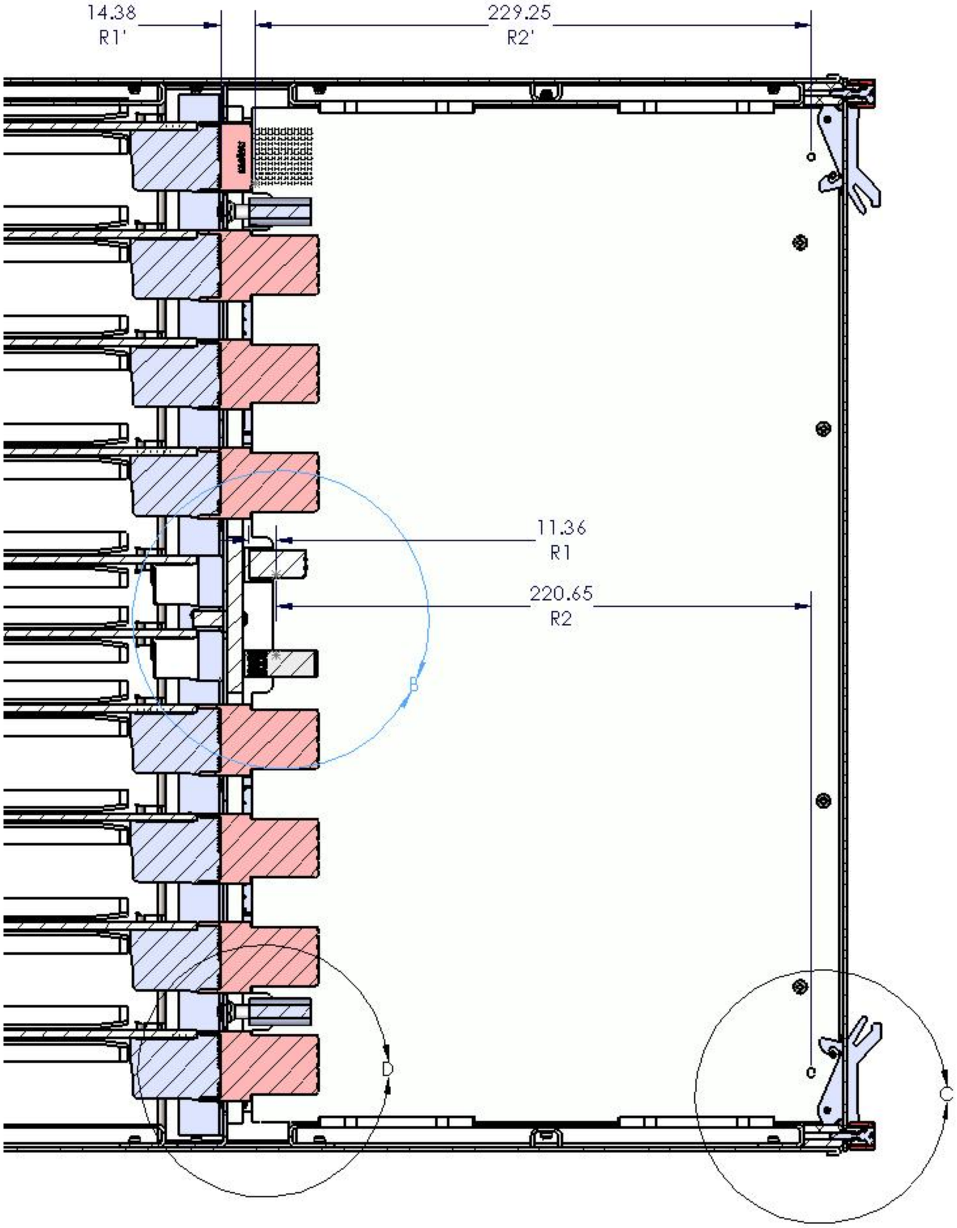


Figure 9: LOOP 2 dimensions

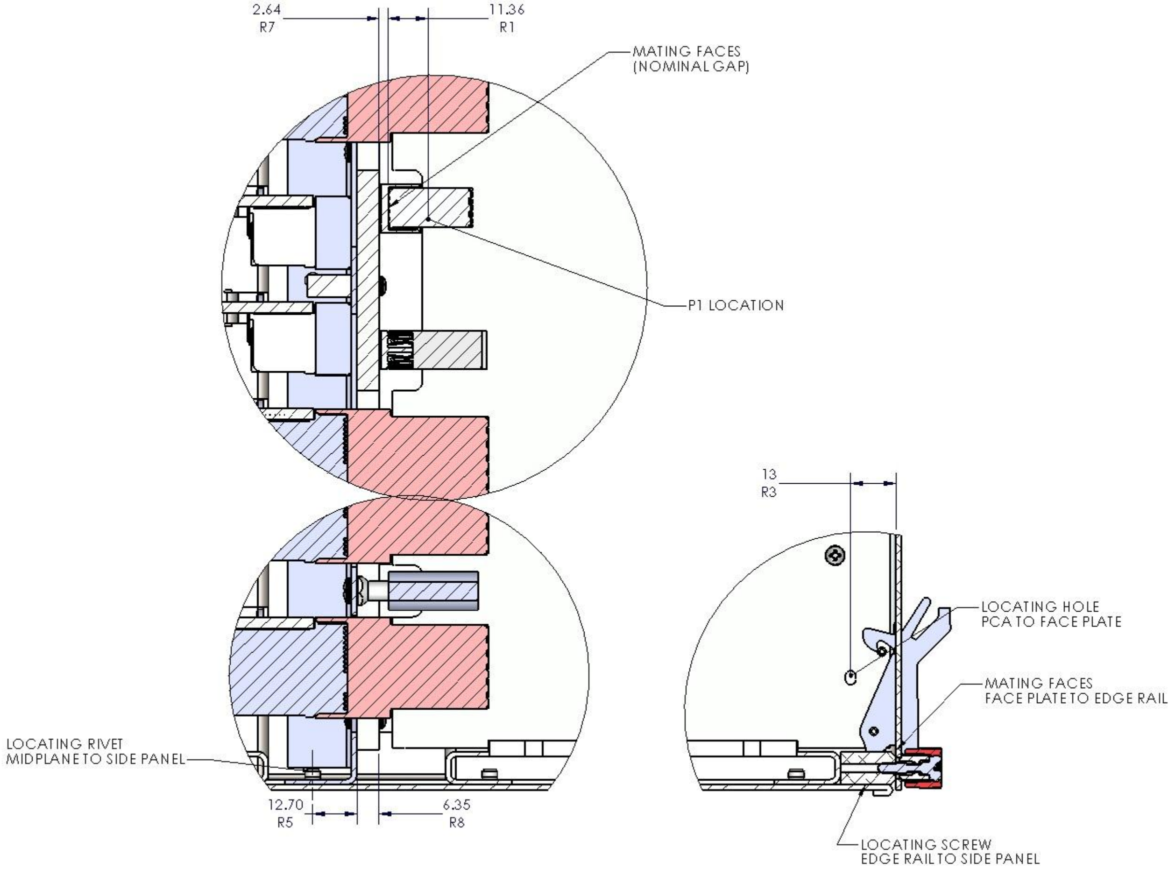


Figure 10: Loop 2 dimensions, close up views

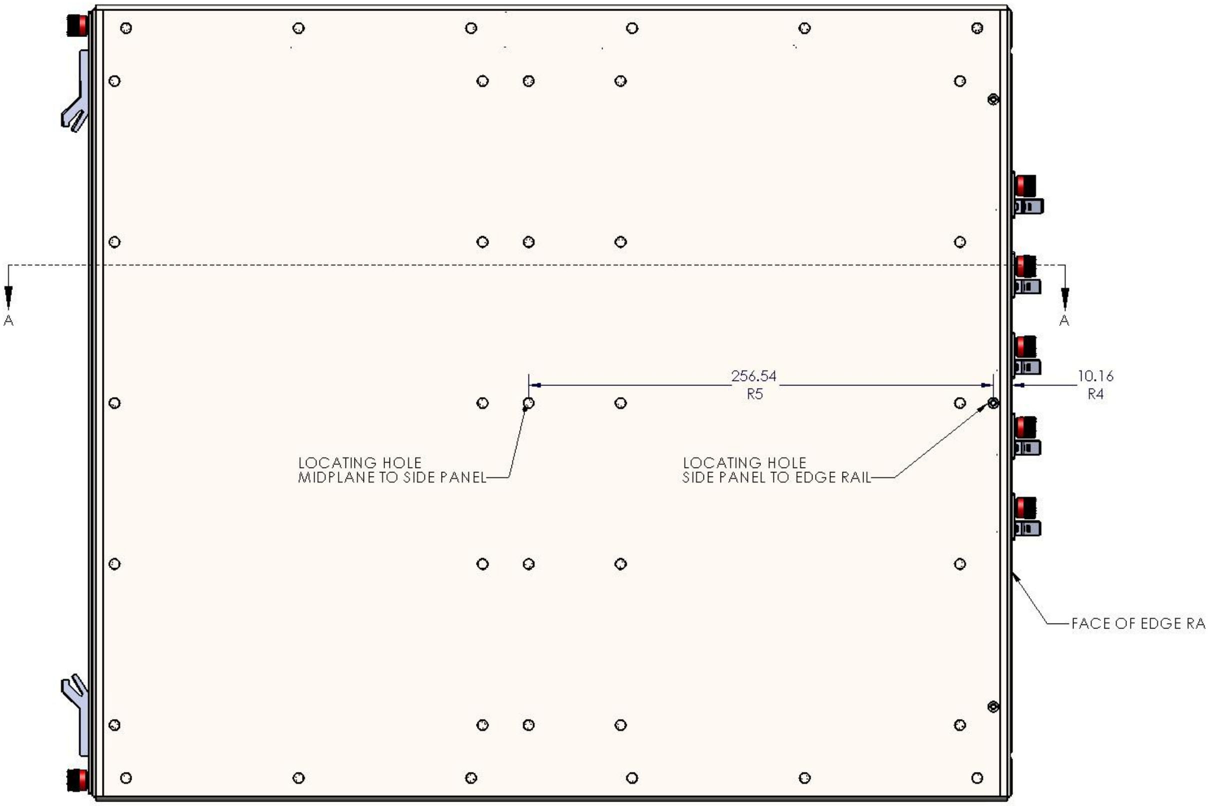


Figure 11: Loop 2, Side Panel dimensions

Tables 4 and 5 show the results of the analysis for Loop 2 with a 0.5mm and 1.0mm nominal gap.

Table 4: LOOP 2 analysis, 0.5mm gap

LOOP 2	Fabric card to Back side of Midplane		Gap=	0.5							
Dim		Nom	Tol +/-	σ Mean Shift	V	Mean Centered Calc	Mean Shifted Calc	Mean Centered σ	Mean Centered σ²	Mean Shifted σ	Mean Shifted σ²
R1	OD RAM connector mating face to P1 location	11.36	0.08	1.5	-1	-11.360	-11.387	0.02667	0.00071	0.01778	0.00032
R2	P1 location to PCB locating hold for face plate	220.65	0.12	1.5	-1	-220.650	-220.690	0.04000	0.00160	0.02667	0.00071
	clearance around locating hole	0.00	0.01	1.5	-1	0.000	-0.003	0.00250	0.00001	0.00167	0.00000
R3	locating hole to locating face on Face Plate	13.00	0.12	1.5	-1	-13.000	-13.040	0.04000	0.00160	0.02667	0.00071
R4	Face of edge rail to mounting hole on side panel	10.16	0.12	1.5	1	10.160	10.120	0.04000	0.00160	0.02667	0.00071
R5	mounting hole on side panel to locating hole for Midplane panel	256.54	0.12	1.5	1	256.540	256.500	0.04000	0.00160	0.02667	0.00071
R6	distance from locating hole to front face of Midplane panel	12.70	0.25	1.5	-1	-12.700	-12.783	0.08333	0.00694	0.05556	0.00309
R7	Connector mating face distance off face of PCA	2.64	0.05	1.5	-1	-2.640	-2.657	0.01667	0.00028	0.01111	0.00012
R8	thickness of Midplane PCB	6.35	0.64	1.5	-1	-6.350	-6.562	0.21167	0.04480	0.14111	0.01991
G	designed gap	0.50	0.00	1.5	1	0.500	0.500	0.00000	0.00000	0.00000	0.00000
			1.50		**Gnom**	**0.500**	-0.001	**0.243**	0.059	0.162	0.026
				Centered Mean				**Shifted Mean**			
	Nominal Gap	0.500		Design Sigma	2.056			Design Sigma	-0.005		
	Sigma	0.243		Probability	1.99%			Probability	50.21%		
	3 sigma	0.730		PPM	19892			PPM	502051		

Table 5: LOOP 2 analysis, 1.0mm gap

LOOP 2	Fabric card to Back side of Midplane		Gap=	1.0							
Dim		Nom	Tol +/-	σ Mean Shift	V	Mean Centered Calc	Mean Shifted Calc	Mean Centered σ	Mean Centered σ²	Mean Shifted σ	Mean Shifted σ²
R1	OD RAM connector mating face to P1 location	11.36	0.08	1.5	-1	-11.360	-11.387	0.02667	0.00071	0.01778	0.00032
R2	P1 location to PCB locating hole for face plate	220.65	0.12	1.5	-1	-220.650	-220.690	0.04000	0.00160	0.02667	0.00071
	clearance around locating hole	0.00	0.01	1.5	-1	0.000	-0.003	0.00250	0.00001	0.00167	0.00000
R3	locating hole to locating face on Face Plate	13.00	0.12	1.5	-1	-13.000	-13.040	0.04000	0.00160	0.02667	0.00071
R4	Face of edge rail to mounting hole on side panel	10.16	0.12	1.5	1	10.160	10.120	0.04000	0.00160	0.02667	0.00071
R5	mounting hole on side panel to locating hole for Midplane panel	256.54	0.12	1.5	1	256.540	256.500	0.04000	0.00160	0.02667	0.00071
R6	distance from locating hole to front face of Midplane panel	12.70	0.25	1.5	-1	-12.700	-12.783	0.08333	0.00694	0.05556	0.00309
R7	Connector mating face distance off face of PCA	2.64	0.05	1.5	-1	-2.640	-2.657	0.01667	0.00028	0.01111	0.00012
R8	thickness of Midplane PCB	6.35	0.64	1.5	-1	-6.350	-6.562	0.21167	0.04480	0.14111	0.01991
G	designed gap	1.00	0.00	1.5	1	1.000	1.000	0.00000	0.00000	0.00000	0.00000
			1.50		**Gnom**	**1.000**	0.499	**0.243**	0.059	0.162	0.026
				Centered Mean				**Shifted Mean**			
	Nominal Gap	1.000		Design Sigma	4.112			Design Sigma	3.079		
	Sigma	0.243		Probability	0.00%			Probability	0.10%		
	3 sigma	0.730		PPM	20			PPM	1039		

With these two analyses (Loop 1 and Loop 2) we have described the tolerance conditions of the typical midplane chassis design in use today. Loop 2 shows that the midplane thickness is the gating factor in determining how large of a nominal gap is required and how much pin wipe can be guaranteed. At

0.5mm, the probability of crashing is 1.99% or 19892PPM, a significant risk. At 1.0mm nominal gap, the probability drops to near zero or 20PPM. The 3 sigma tolerance variation on the rear side of the midplane increases from 0.421mm to 0.730mm. Subtracted from the total pin wipe (2.0mm) leaves 1.270mm available and subtracting a nominal gap of 0.5mm then estimates the guaranteed pin wipe would be 0.77mm. Today's chassis designs solve this problem in a variety of ways. One is to reduce the midplane thickness. Changing the midplane from 6.35 to 3.18mm thick will improve the probability to 0.09% (885PPM). Another method is to use fixtures during the assembly of the chassis to set the edge guide panels a fixed distance from the front and rear face of the midplane. This takes a number of the tolerances out of the loop and tightens the overall tolerance variation.

LOOP 3

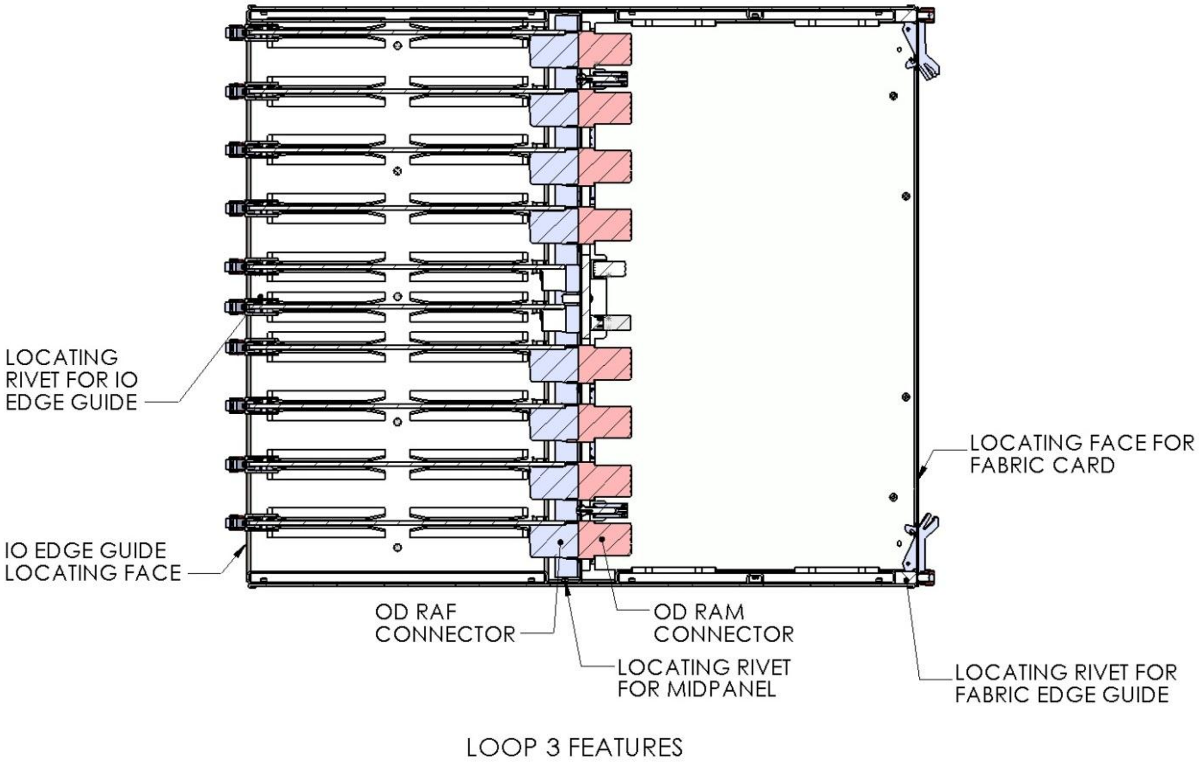


Figure 12: Loop 3 features

Mating of the OD Impact connectors is defined by Loop 3. The dimension loop is composed of a partial combination of dimensions from Loop 1 and 2. From Loop 1, the dimensions are from the OD RAF connector face on the IO PCB through the face plate to the Edge guide panel and top cover and end at the locating hole for the midplane panel. Skip any dimensions related to the Midplane PCB and go to Loop 2 dimensions. Continue with the locating hole for the side panel and travelling backwards to the edge guide rail then face plate of the Fabric card and end with the mating face of the OD RAM connector. See the dimension loop below.

Loop 3: IO to Fabric card mating connectors.

D1 = OD RAF connector mating face to P1 location

D2 = P1 location to PCB locating hole for Face Plate. Include hole to pin clearance in tolerance.

D3 = locating hole to locating face on face plate. Face is fastened to edge guide

D4 = Face of edge guide to locating hole for top panel

D5 = locating hole for edge guide to locating hole for midplane in top panel

Transition = Positional shift from top flange of midplane to the side flange. The dimension in the study is zero, but there is a tolerance associated in the transition from hole to hole as the dimensional loop moves from the top to the side panel.

R5 = mounting hold on side panel to locating hole for Midplane panel.

R4 = Face of edge rail to mounting hole on side panel

R3 = locating hole to locating face on face plate. Face is fastened to edge rail

R2' = P1 location to PCB locating hole for Face Plate. Include hole to pin clearance in tolerance.

R1' = OD RAM connector mating face to P1 location

The actual dimension values for R1' and R2' (shown in Figure 9) change to represent the OD RAM connector instead of the Midplane connector, but the tolerances remain the same. This loop has the most dimensions and thus will have the most tolerances to accommodate, though the computed probability is comparable to Loop 1. The probability of bottoming out is 0.09% (870 PPM). The minimum pin wipe is computed as 2.0-.5-.489 = 1.011mm.These analyses thus demonstrate that designing an OD connector system will be just as reliable as the typical midplane chassis design in production today.

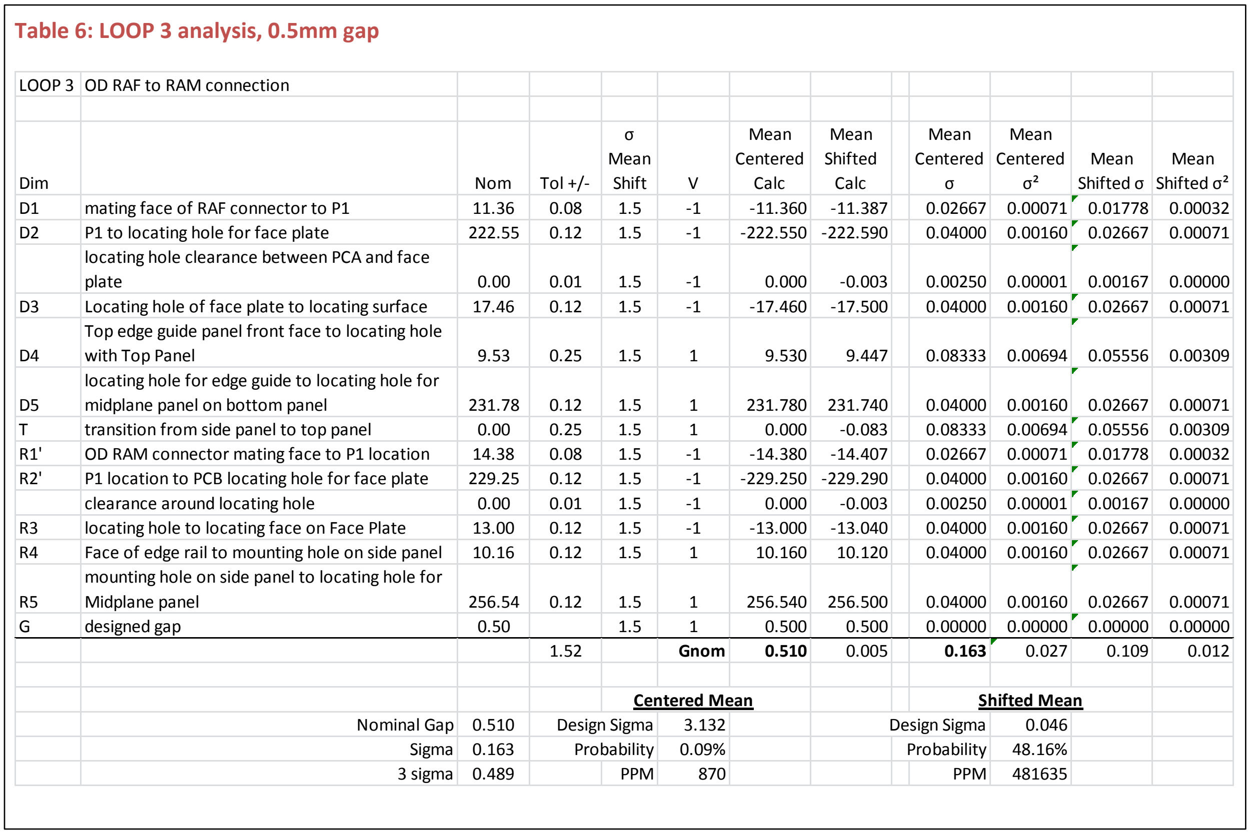


Table 6: LOOP 3 analysis, 0.5mm gap

LOOP 3	OD RAF to RAM connection										
Dim		Nom	Tol +/-	σ Mean Shift	V	Mean Centered Calc	Mean Shifted Calc	Mean Centered σ	Mean Centered σ²	Mean Shifted σ	Mean Shifted σ²
D1	mating face of RAF connector to P1	11.36	0.08	1.5	-1	-11.360	-11.387	0.02667	0.00071	0.01778	0.00032
D2	P1 to locating hole for face plate	222.55	0.12	1.5	-1	-222.550	-222.590	0.04000	0.00160	0.02667	0.00071
	locating hole clearance between PCA and face plate	0.00	0.01	1.5	-1	0.000	-0.003	0.00250	0.00001	0.00167	0.00000
D3	Locating hole of face plate to locating surface	17.46	0.12	1.5	-1	-17.460	-17.500	0.04000	0.00160	0.02667	0.00071
D4	Top edge guide panel front face to locating hole with Top Panel	9.53	0.25	1.5	1	9.530	9.447	0.08333	0.00694	0.05556	0.00309
D5	locating hole for edge guide to locating hole for midplane panel on bottom panel	231.78	0.12	1.5	1	231.780	231.740	0.04000	0.00160	0.02667	0.00071
T	transition from side panel to top panel	0.00	0.25	1.5	1	0.000	-0.083	0.08333	0.00694	0.05556	0.00309
R1'	OD RAM connector mating face to P1 location	14.38	0.08	1.5	-1	-14.380	-14.407	0.02667	0.00071	0.01778	0.00032
R2'	P1 location to PCB locating hole for face plate	229.25	0.12	1.5	-1	-229.250	-229.290	0.04000	0.00160	0.02667	0.00071
	clearance around locating hole	0.00	0.01	1.5	-1	0.000	-0.003	0.00250	0.00001	0.00167	0.00000
R3	locating hole to locating face on Face Plate	13.00	0.12	1.5	-1	-13.000	-13.040	0.04000	0.00160	0.02667	0.00071
R4	Face of edge rail to mounting hole on side panel	10.16	0.12	1.5	1	10.160	10.120	0.04000	0.00160	0.02667	0.00071
R5	mounting hole on side panel to locating hole for Midplane panel	256.54	0.12	1.5	1	256.540	256.500	0.04000	0.00160	0.02667	0.00071
G	designed gap	0.50		1.5	1	0.500	0.500	0.00000	0.00000	0.00000	0.00000
			1.52		**Gnom**	**0.510**	0.005	**0.163**	0.027	0.109	0.012
				Centered Mean				**Shifted Mean**			
	Nominal Gap	0.510		Design Sigma	3.132			Design Sigma	0.046		
	Sigma	0.163		Probability	0.09%			Probability	48.16%		
	3 sigma	0.489		PPM	870			PPM	481635		

LATERAL CONNECTOR MATING

Now, turn your attention to the other two directional loops (X and Y). These follow the traditional design parameters and considerations. The tolerance stacks for the traditional midplane design and the OD design are similar. It is instructive to go through the tolerance loops so you can see how this is done and apply it to your particular design.

Here is a partial list of cage design choices.

The main potential for a large variability in this analysis comes from the potential bowing of the PCB, especially if it is a large card or has heavy components installed. Designers will take typical measures to keep the board relatively flat by using a thicker PCB or adding mechanical stiffening to the board. In the case of a wide board, the designer also has the option of using integrated guide pins in the OD Connector or adding a standalone guide pin in the center of the board for additional support and guidance. These are choices for the designer to make.

Are the guide pins mounted to the midplane sheet metal panel or the midplane PCB? Does it make a difference? Does it make a difference if you use integrated or stand-alone guide pins? All of these have a minimal impact on the tolerance question. This will be shown in the analysis below. As the cards come together, there is a series of transitions; which components provide the guidance and locating features for proper mating. The first to mate are the guide pins, and they have the largest range of clearance to engage. Therefore the small tolerance associated with the mounting style has a minimal impact. See the analysis below for details. As the guide pins direct the cards into alignment, the tallest connectors then begin to engage and take over the locating function since they have a tighter clearance for mating. Finally, the shorter connectors are engaged. Since guide pins and connector mating has been successfully used in the industry, we can conclude that with proper design, if the taller connectors mate properly then all the connectors will mate without issue. There isn't a lot of clearance in the guide receptacles, but it is enough to allow all of the connectors to float and mate within their respective tolerance fields. Part of this comes from the compliance of the connector systems. From this we can assume if the connectors are close enough to mate within their tolerance system, then after mating, the guide pins are no longer the sole source in controlling the location of components, but just another set of components in the total connector system which has reached a positional equilibrium of clearances and compliance.

The ortho direct connectors allow you to remove the midplane from the design around this bank of connectors. But it is not a requirement. If you want to keep the structural integrity of the midplane so it can be used for the guide pins (to reduce the tolerance loop), you could only remove a small windows around all the OD connectors to pass thru and leave the rest of the board intact (see picture). The main implication would be that you could not take advantage of a straight thru air flow from front to back but would stay with the direction flow (in the case from top to bottom for the front cards and side to side for the rear cards). Most chassis are designed in a manner to handle air flow with a solid midplane today. You would still gain the benefit of direct electrical path from card to card that the OD connector provides. So you could use an existing chassis design and just change the boards to create an OD design. The mechanical chassis and cooling components would not have to change.

Pictured below is the T profile used in the reference design, a full panel window design, and a pass thru only design as described above. One assumption in all these designs is the need for the IO, Management, and Fabric cards to connect to the midplane for power and for some signal management from the Management card to the IO and Fabric cards. In the reference design, it would also be possible for designers to consider using OD connectors between the Management and Fabric cards. This would eliminate the midplane thickness in the tolerance loop analysis for all but the power connectors in the midplane to the Fabric cards. Since power connectors generally have a longer minimum pin wipe, this is another way to improve the minimum pin wipe for the signal Impact connectors.

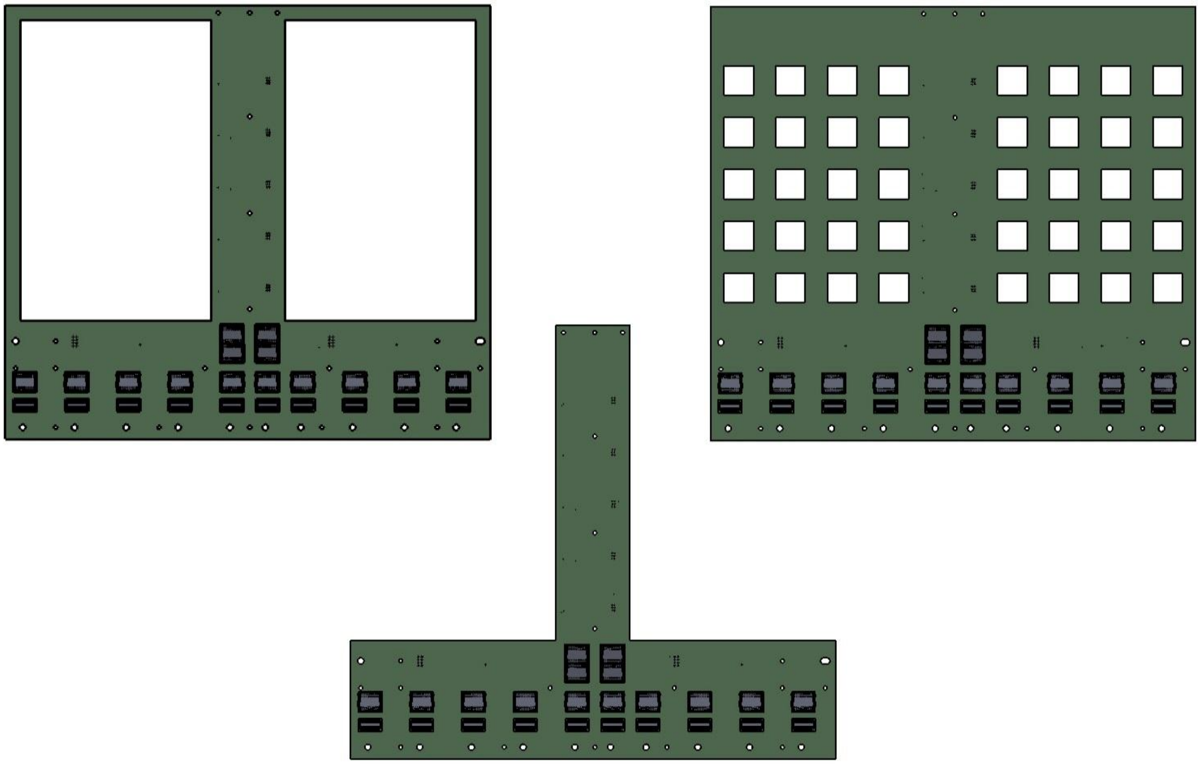
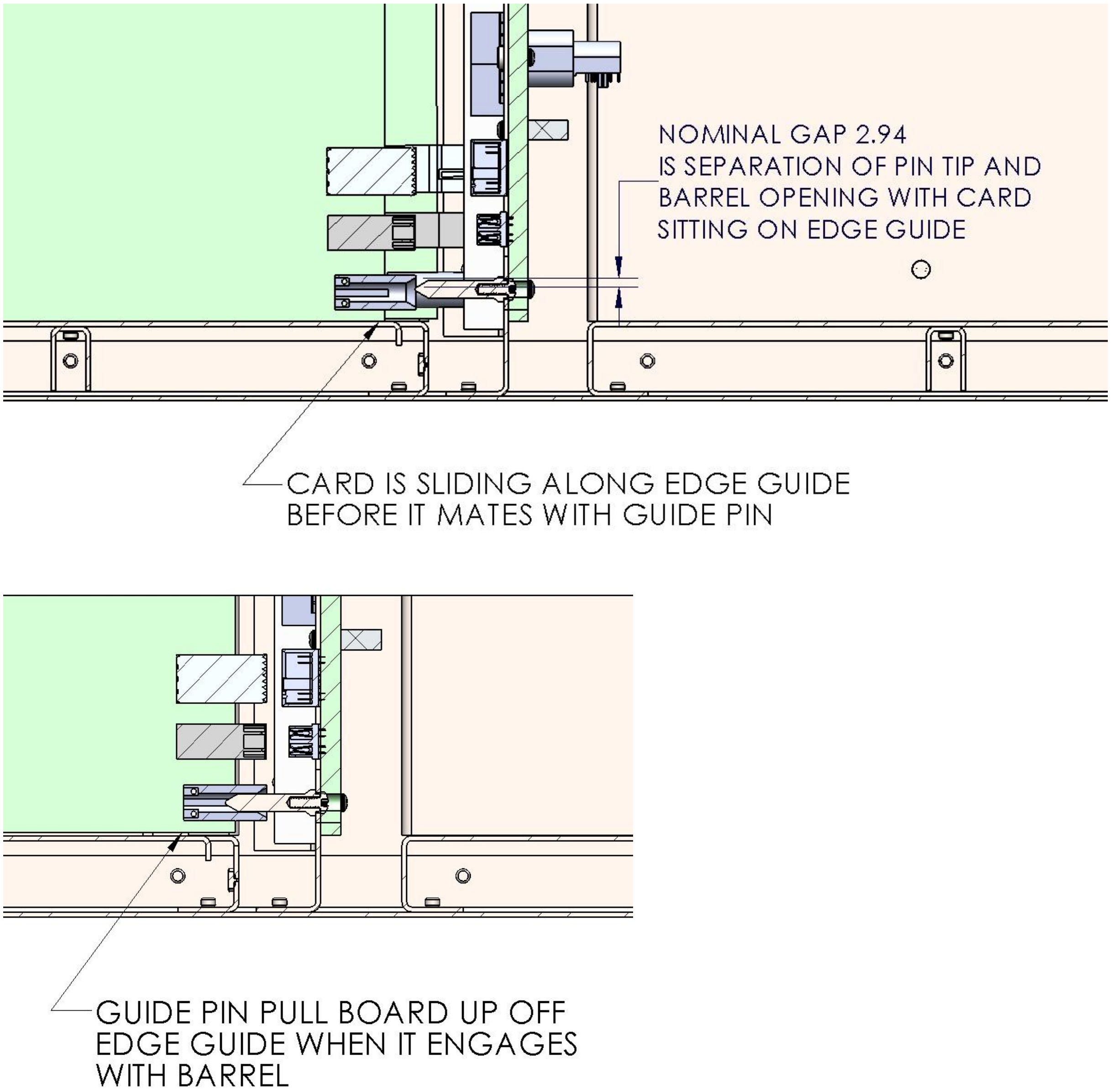


Figure 13: Midplane design options

GUIDE PIN ENGAGEMENT

In the X or Y direction, the midplane panel is the starting reference. The engagement tolerances change as the boards come together. The first engagement is the guide pins. In this tolerance loop, none of the other components are engaged and thus don't matter at this point.

The design will have the pin and barrel center lines in alignment. The nominal gap is the amount of clearance between the tip diameter of the pin and the outer barrel diameter of the lead-in cone (see Fig 15). In the Y direction, gravity will pull the board down so it slides along the edge guide panel. This bias downwards results in the nominal gap being asymmetrical for the pin entering the mating barrel; the smaller side of the gap is used for analysis. When the pin slides into the barrel, the card will be lifted off of the edge guide. In most cases, the back edge of the card will still be sliding along the edge guide, resulting is a small amount of tilt to the card. The result is that the lower connectors will begin to engage before the top connectors, but the nominal gap at each connector is not changed so all connectors will mate appropriately. Eventually the card is completely injected at both top and bottom and the back edge of the card will lift off the edge guide. Some cage design reduce any loading or stress on the connectors during injection by putting guide pins in the face of the chassis as part of the injection system, lifting both sides of the card at the same time. The clearance in the X direction between the edge guide channels is a similar situation and the card will tend to ride to one side or the other depending on how the user is inserting the card. Whether the edge guide is designed to capture the card or a sheet metal panel under the card is a choice the designer can make. Both have the same effect on the tolerances. To mate successfully, the gap must remain greater than zero in both directions.



NOMINAL GAP 2.94
IS SEPARATION OF PIN TIP AND
BARREL OPENING WITH CARD
SITTING ON EDGE GUIDE

CARD IS SLIDING ALONG EDGE GUIDE
BEFORE IT MATES WITH GUIDE PIN

GUIDE PIN PULL BOARD UP OFF
EDGE GUIDE WHEN IT ENGAGES
WITH BARREL

Figure 14: Guide Pin engagement sequence

The reference design allows for 1mm or more of clearance between the cards and the side panels that form the edge guides. Even so, there is nearly 3mm of tolerance allowed for the pin and barrel to mate. Table 7 shows this analysis.

Starting from the origin of the Midplane support, this design distance to the guide pin and the mating barrel is the same. For simplicity, D4 uses this same origin location for the PCB.

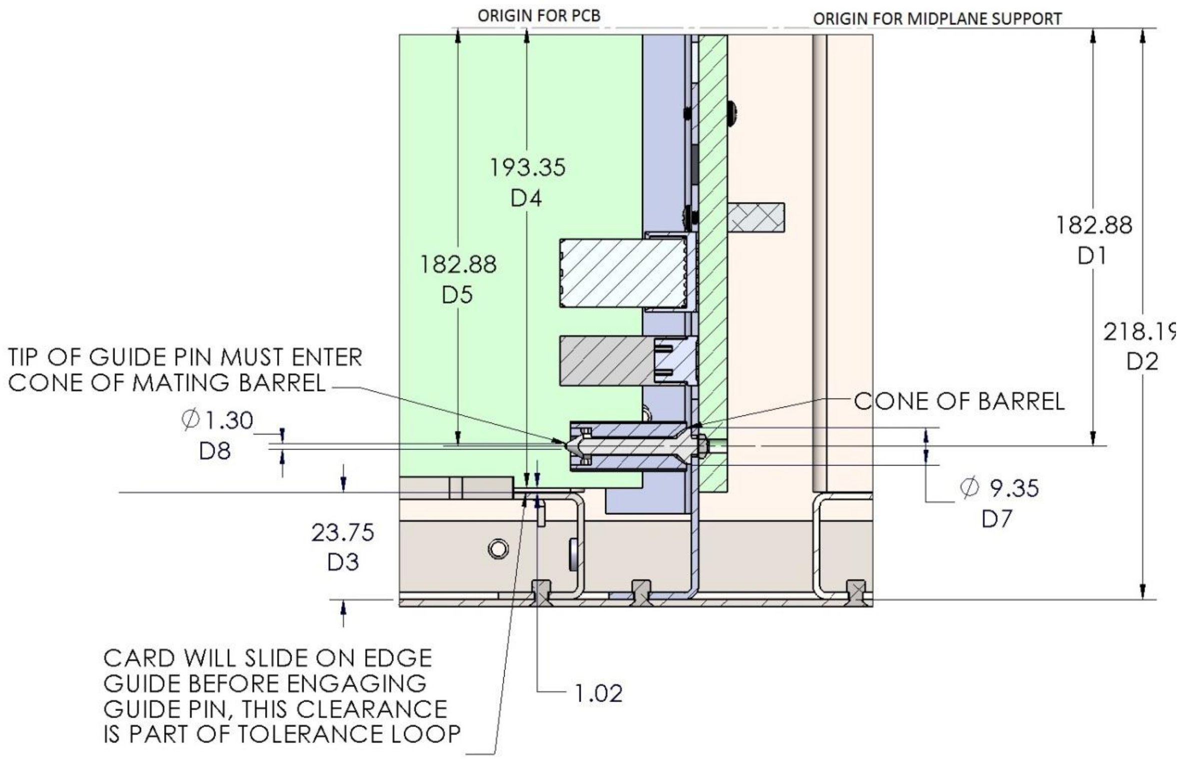


Figure 15: Guide Pin engagement loop

D1 = Origin to guide pin location, the tolerance represents the transition from the origin hole around a bend and location of the hole on the midplane support face.

D2 = Origin to outside fold that mates with the bottom panel

D3 = height of the double folded edge guide panel

D4 = card edge to PCB origin

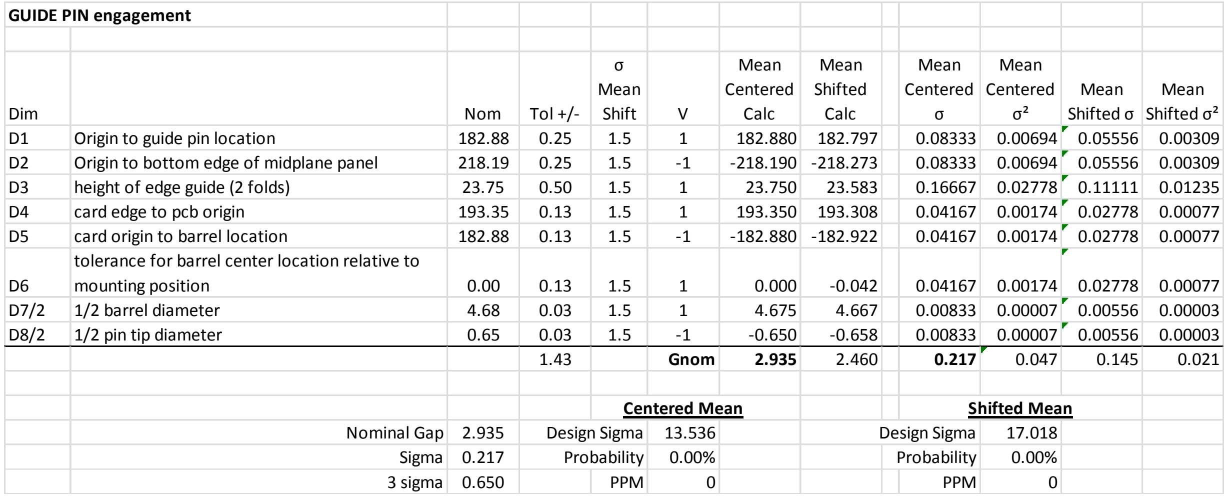
D5 = card origin to barrel location

D6 = barrel location to barrel center = 0

D7 = ½ barrel diameter

D8 = ½ Pin tip diameter

Table 7: Guide Pin engagement



GUIDE PIN engagement											
Dim		Nom	Tol +/-	σ Mean Shift	V	Mean Centered Calc	Mean Shifted Calc	Mean Centered σ	Mean Centered σ²	Mean Shifted σ	Mean Shifted σ²
D1	Origin to guide pin location	182.88	0.25	1.5	1	182.880	182.797	0.08333	0.00694	0.05556	0.00309
D2	Origin to bottom edge of midplane panel	218.19	0.25	1.5	-1	-218.190	-218.273	0.08333	0.00694	0.05556	0.00309
D3	height of edge guide (2 folds)	23.75	0.50	1.5	1	23.750	23.583	0.16667	0.02778	0.11111	0.01235
D4	card edge to pcb origin	193.35	0.13	1.5	1	193.350	193.308	0.04167	0.00174	0.02778	0.00077
D5	card origin to barrel location	182.88	0.13	1.5	-1	-182.880	-182.922	0.04167	0.00174	0.02778	0.00077
D6	tolerance for barrel center location relative to mounting position	0.00	0.13	1.5	1	0.000	-0.042	0.04167	0.00174	0.02778	0.00077
D7/2	1/2 barrel diameter	4.68	0.03	1.5	1	4.675	4.667	0.00833	0.00007	0.00556	0.00003
D8/2	1/2 pin tip diameter	0.65	0.03	1.5	-1	-0.650	-0.658	0.00833	0.00007	0.00556	0.00003
			1.43		**Gnom**	**2.935**	2.460	**0.217**	0.047	0.145	0.021
					Centered Mean				**Shifted Mean**		
	Nominal Gap	2.935	Design Sigma	13.536			Design Sigma	17.018			
	Sigma	0.217	Probability	0.00%			Probability	0.00%			
	3 sigma	0.650	PPM	0			PPM	0			

ORTHO CONNECTOR ENGAGEMENT

Once the guide pins are mated, then the card is lifted up off the chassis edge guide and is supported by the guide pins. The previously mentioned paper from Molex goes into considerable detail about the connector to connector mating analyses. (Appendix A)

The reference design is slightly different from the traditional construction because the guide pins are placed in the chassis midplane sheet metal panel instead of in the midplane PCB. By doing this, an extra tolerance is included in the dimensional stack and represents a worse case situation for the analysis. It will be the designer's choice where to install the guide pin and whether to use independent pins as the reference design, or integrated pins available in the OD connector line. Look at this tolerance loop construction as an example you can follow for your designs. The below analysis demonstrates that the OD connectors are similar to traditional midplane connector engagement.

The guide pin is the origin for this analysis. The mating connectors are the IO RAF and FABRIC RAM OD connectors.

As mentioned above, the guide pins are located on the chassis midplane panel, not the midplane PCB, so the dimensional loop includes the transition from the panel to the PCBs of both cards.

D1 = Barrel center to its locating feature. The clearance between the pin and the barrel (1/2 diameter difference) should be subtracted from this dimension as the board will be biased by gravity downwards, however the same will be true of the Fabric card, so the net is a zero change in gap. The tolerance variance does need to be included in both dimensions.

D2 = Barrel locating feature to the PCB origin.

D3 = IO PCB Origin to P1 of OD RAF connector

D4 = P1 of OD RAF connector to lead in edge. Figure 17 shows that the lead in gap is slightly different at each end of the connector. The smaller gap has been chosen for this analysis.

D5 = Guide pin to guide pin location on the midplane panel. One is on each side of the panel.

D6 = Guide pin centerline to the top face of the PCB.

D7 = distance from the PCB face which is the mounting face of the OD RAM connector to the lead in edge of the connector. That completes the loop

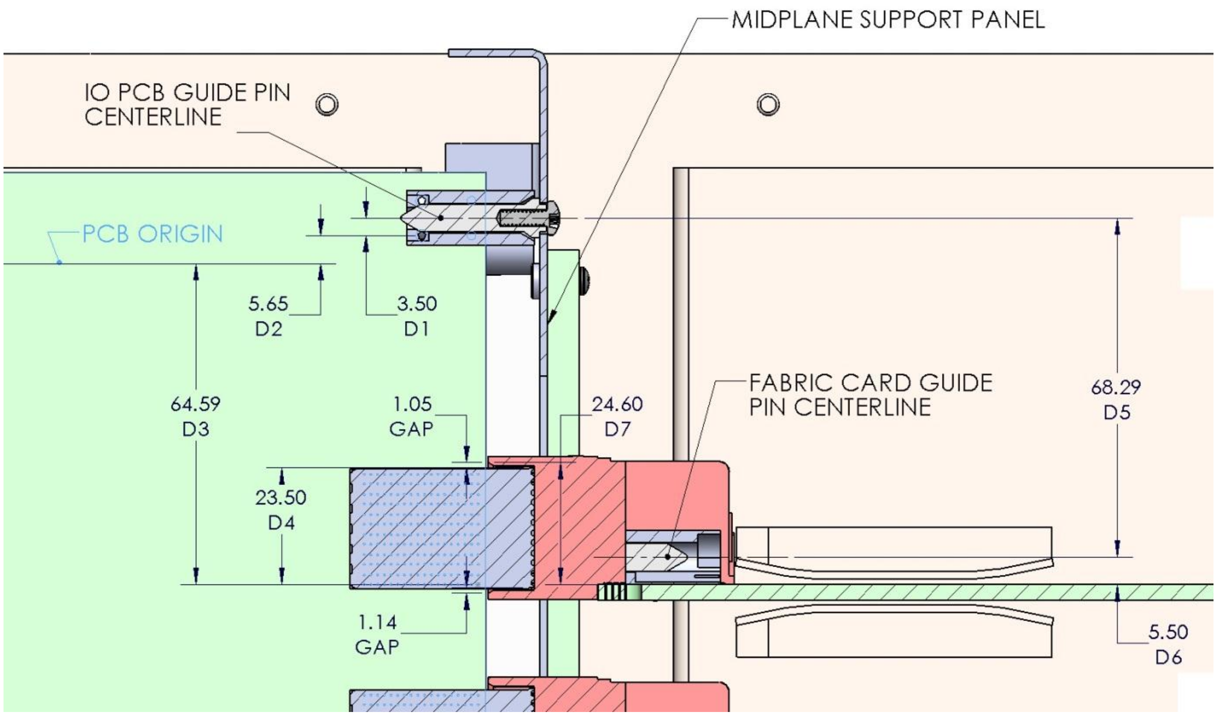


Figure 16: Ortho Direct LOOP

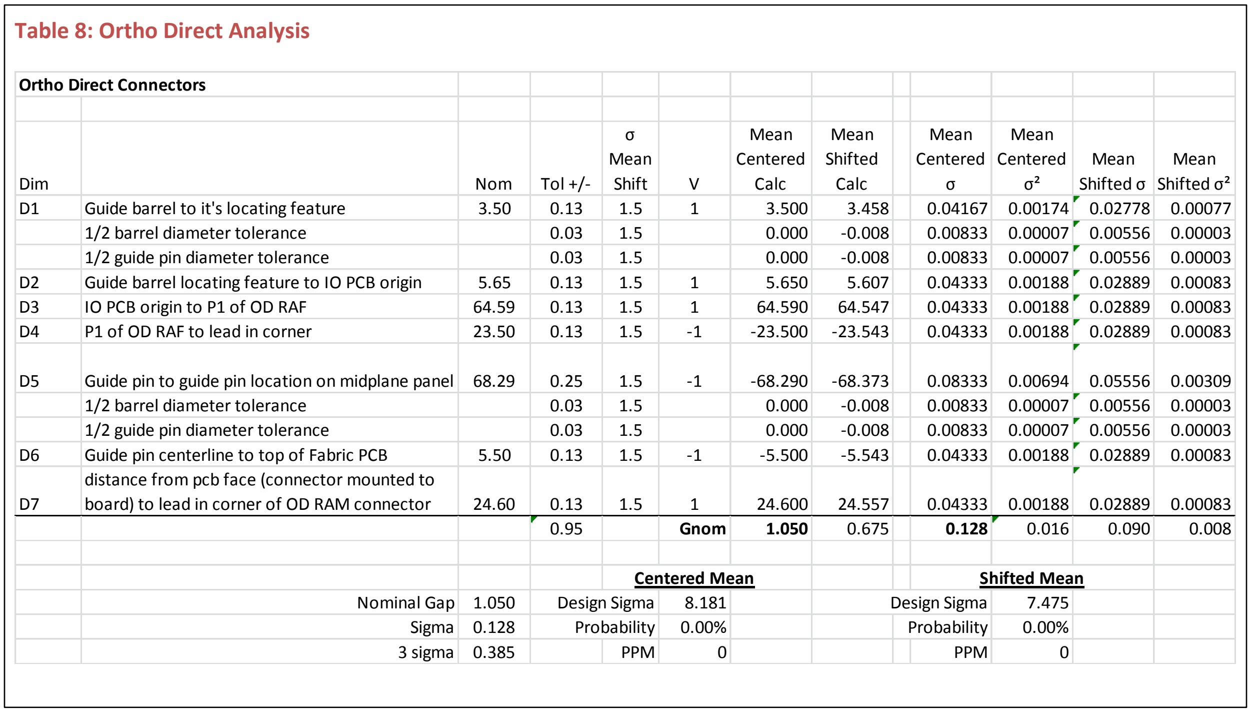


Table 8: Ortho Direct Analysis

Ortho Direct Connectors

Dim		Nom	Tol +/-	σ Mean Shift	V	Mean Centered Calc	Mean Shifted Calc	Mean Centered σ	Mean Centered σ²	Mean Shifted σ	Mean Shifted σ²
D1	Guide barrel to it's locating feature	3.50	0.13	1.5	1	3.500	3.458	0.04167	0.00174	0.02778	0.00077
	1/2 barrel diameter tolerance		0.03	1.5		0.000	-0.008	0.00833	0.00007	0.00556	0.00003
	1/2 guide pin diameter tolerance		0.03	1.5		0.000	-0.008	0.00833	0.00007	0.00556	0.00003
D2	Guide barrel locating feature to IO PCB origin	5.65	0.13	1.5	1	5.650	5.607	0.04333	0.00188	0.02889	0.00083
D3	IO PCB origin to P1 of OD RAF	64.59	0.13	1.5	1	64.590	64.547	0.04333	0.00188	0.02889	0.00083
D4	P1 of OD RAF to lead in corner	23.50	0.13	1.5	-1	-23.500	-23.543	0.04333	0.00188	0.02889	0.00083
D5	Guide pin to guide pin location on midplane panel	68.29	0.25	1.5	-1	-68.290	-68.373	0.08333	0.00694	0.05556	0.00309
	1/2 barrel diameter tolerance		0.03	1.5		0.000	-0.008	0.00833	0.00007	0.00556	0.00003
	1/2 guide pin diameter tolerance		0.03	1.5		0.000	-0.008	0.00833	0.00007	0.00556	0.00003
D6	Guide pin centerline to top of Fabric PCB	5.50	0.13	1.5	-1	-5.500	-5.543	0.04333	0.00188	0.02889	0.00083
D7	distance from pcb face (connector mounted to board) to lead in corner of OD RAM connector	24.60	0.13	1.5	1	24.600	24.557	0.04333	0.00188	0.02889	0.00083
			0.95		**Gnom**	**1.050**	0.675	**0.128**	0.016	0.090	0.008
					Centered Mean				**Shifted Mean**		
	Nominal Gap	1.050		Design Sigma	8.181			Design Sigma	7.475		
	Sigma	0.128		Probability	0.00%			Probability	0.00%		
	3 sigma	0.385		PPM	0			PPM	0		

The last thing to mention, this is an opportunity to include a tolerance for sagging or bowing of the card. The designer can determine his design criterion, or use this analysis to play what-if scenarios to determine what range of deflection the design can tolerate.

The analysis shows a nominal gap of 1.05mm and a 3 sigma calculation of .40mm, leaving 0.65mm available for potential sagging or bowing of the board. This suggests that a center guide pin or integrated guide pins in the OD connectors would be a necessary requirement for minimal risk of crashing the connectors for wide or heavy boards.